JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP), for Serial NOR Flash

JESD216

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SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP), FOR SERIAL NOR FLASH

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Foreword

This document was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman.

The intended audience is serial NOR flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI:

"The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward compatible software support for the specified flash device families. It allows flash vendors to standardize their existing interfaces for long-term compatibility".

The current SFDP document defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Additional parameter headers and tables can be specified by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP), FOR SERIAL NOR FLASH

(From JEDEC Board Ballot JCB-11-22, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory).

1 Scope

This standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header and basic flash parameter table is mandatory. Additional flash vendor-defined headers and tables are optional.

The read instruction protocol using various I/O modes and standard clock rate are specified. The device operating voltage is not specified.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

(There are no normative documents at this time, but this space is reserved for future use to be in compliance with JEDEC document standards)

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply:

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

DTR: Double Transfer Rate. Opcode, address, and/or data may be input or output on both the rising and falling edges of the clock.

DWORD: Four consecutive 8-bit bytes used as the basic 32-bit building block for headers and parameter tables.

3 Terms and definitions (cont'd)

Instruction: The combination of the opcode, address, and dummy cycles used to issue a command to the serial flash.

Mode Bits: Optional control bits that follow the address bits. These bits are driven by the system controller if they are specified.

Wait States: Required dummy clock cycles after the address bits or optional mode bits.

(x-y-z): I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

4 Read SFDP Instruction Protocol

4.1 Opcode

The Read SFDP instruction code is 0x5A.

4.2 Address

Indicates the starting read location in the SFDP area and is always expressed as a 24-bit address.

4.3 Dummy cycles (wait states)

Following the address, eight dummy clocks (8 wait states) are required before valid data is clocked out.

4.4 Clock Rate

SFDP compliant devices must support 50 MHz operation for the Read SFDP instruction (opcode 0x5A). Devices may support a wider frequency range, but a controller can always run SFDP cycles at 50 MHz or less and get valid results.

4.5 Instruction Input Modes

The Read SFDP instruction can be used with device supported modes of (1-1-1), (2-2-2), or (4-4-4), but the opcode (0x5A), address (24 bits), eight dummy clocks (8 wait states), and 50 MHz requirements remain the same.

4.5 Instruction Input Modes (cont'd)

4.5.1 Read SFDP (1-1-1) Mode

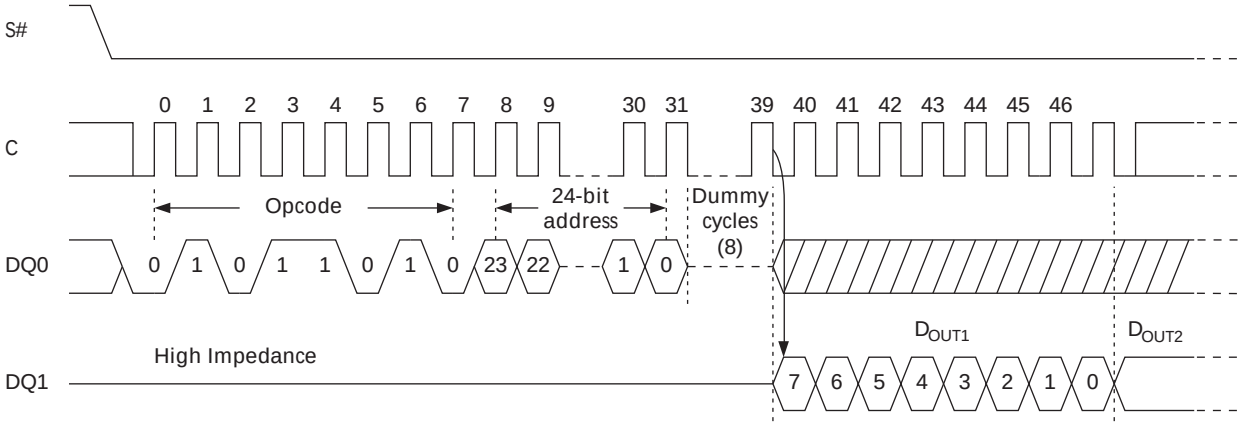

Figure 1 — Read SFDP (1-1-1) Mode Timing Diagram

4.5.2 Read SFDP (2-2-2) Mode

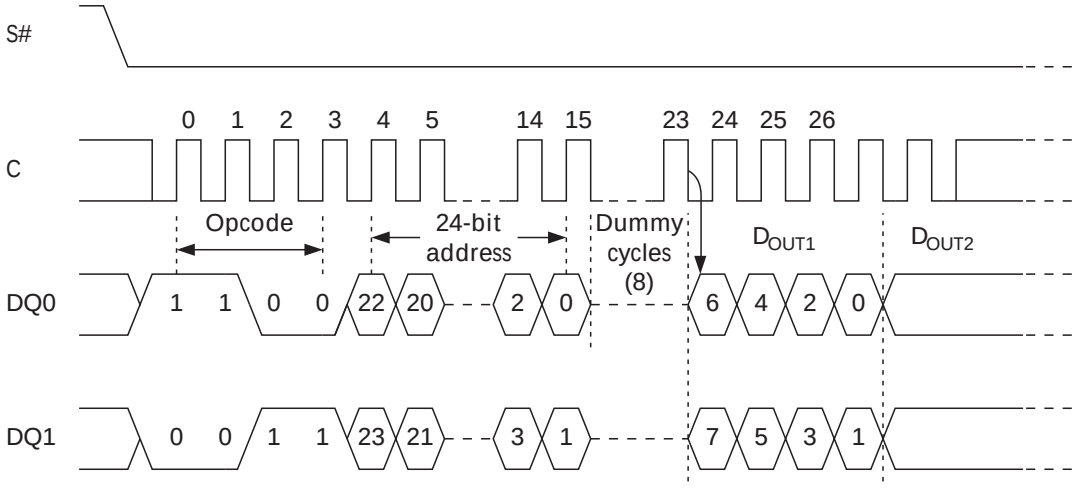

Figure 2 — Read SFDP (2-2-2) Mode Timing Diagram

4.5 Instruction Input Modes (cont'd)

4.5.3 Read SFDP (4-4-4) Mode

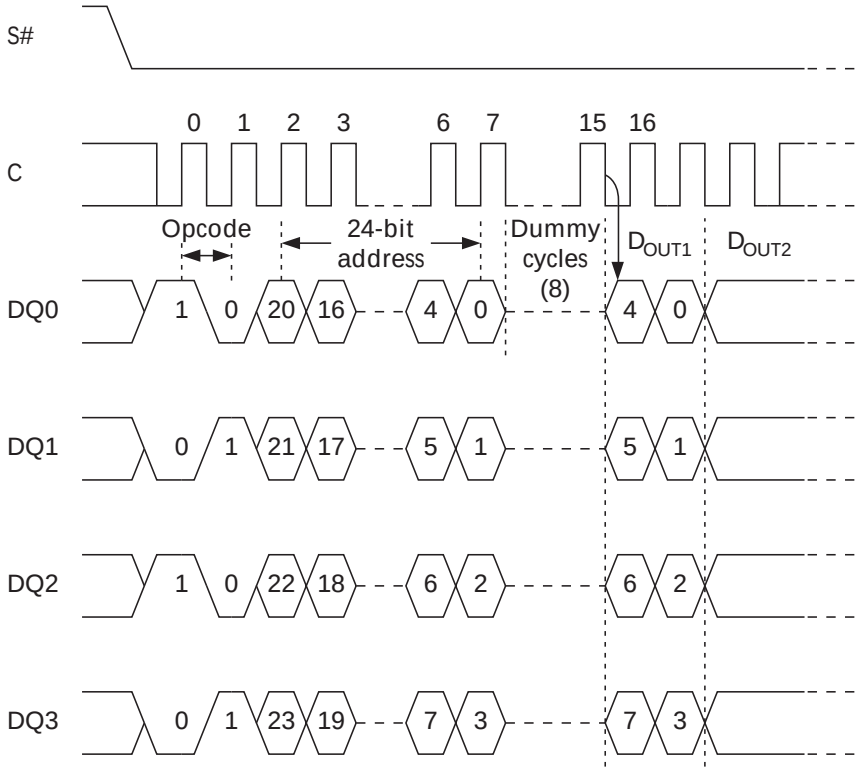

Figure 3 — Read SFDP (4-4-4) Mode Timing Diagram

5 Read SFDP Behavior

5.1 Security

For security reasons, the SFDP and flash memory address ranges must never overlap. Addresses beyond the end of the SFDP tables must not alias into the flash memory. Regardless of the implementation, writes to SFDP tables must be permanently disabled after manufacturing.

5.2 Reset and Hold Functions

Functionality will be available during the Read SFDP instruction if the memory device supports these features.

5.3 Burst Wraps

Not supported with the Read SFDP instruction, even when a memory device defaults to Read Wrap mode. Only continuous reads are supported with the Read SFDP instruction.

5.4 SFDP Address Boundary Wrap

Device behavior when the Read SFDP instruction crosses the SFDP structure boundary is not defined except for the security restriction specified in 5.1. There is no requirement for the address counter to wrap back to the beginning of the structure and the data read after that point is not specified.

5.5 Reserved SFDP Locations

The content of reserved SFDP locations (memory within the SFDP address space that has not yet been defined or used) is not specified, but recommended to be all 0xFF.

6 SFDP Database

6.1 SFDP Overall Header Structure

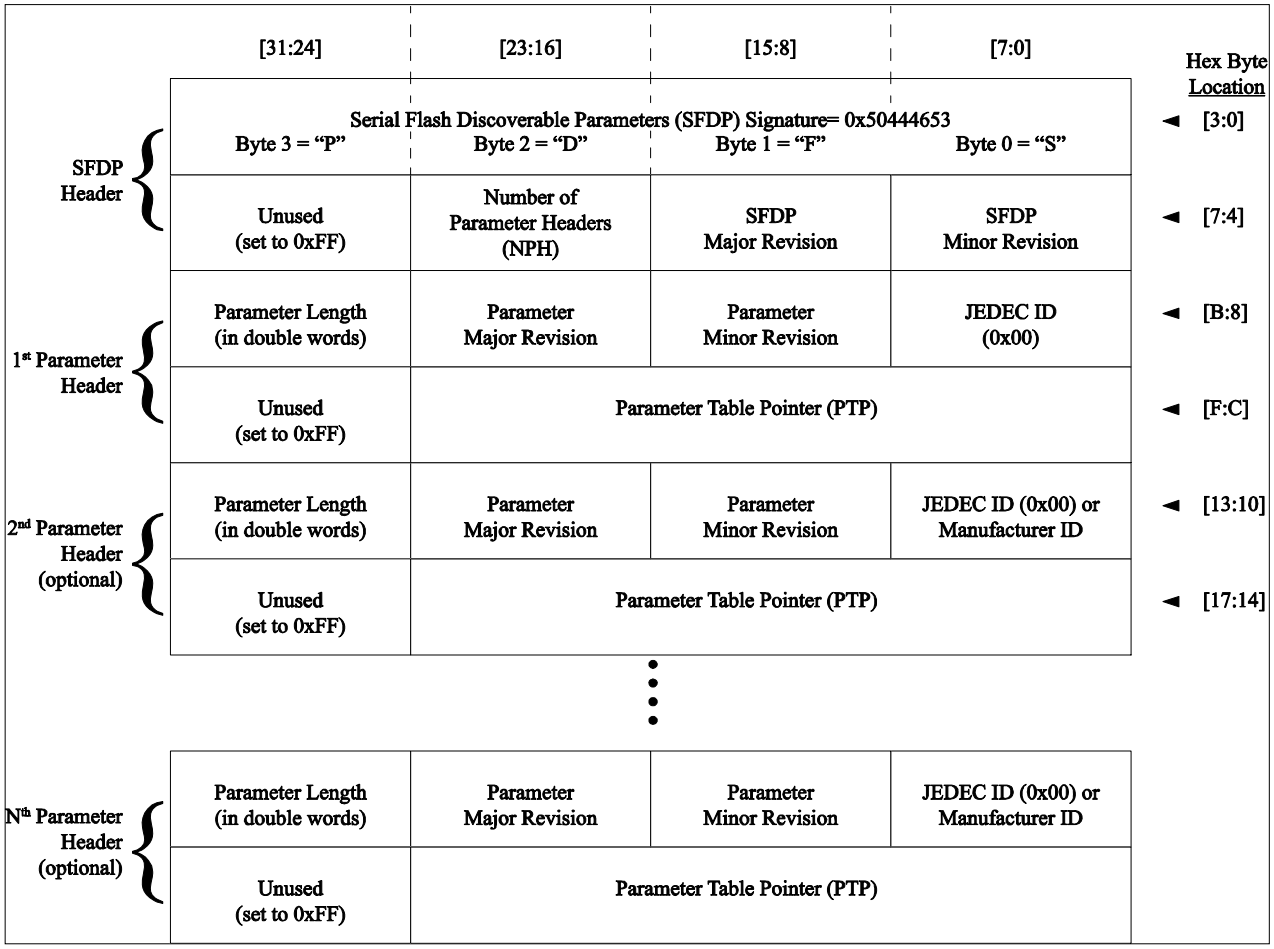

Figure 4 — Overall Header Structure

6.2 SFDP Header

The SFDP Header is located at address 0x000000 of the SFDP data structure. It identifies the SFDP Signature, the number of parameter headers, and the SFDP revision numbers.

6.2.1 SFDP Header: 1st DWORD

Bits	Description
31:0	**SFDP Signature** Allows a user to know that the information is valid. Signature[31:0]: 0x50444653

6.2 SFDP Header (cont'd)

6.2.2 SFDP Header: 2nd DWORD

Bits	Description
31:24	**Unused** Contains 0xFF and can never be changed.
23:16	**Number of Parameter Headers (NPH)** Specifies the number of parameter headers in the SFDP data structure. This number is 0-based. Therefore, 0 indicates 1 parameter header. This number must be revised by a vendor or JEDEC when a new parameter header is added
15:8	**SFDP Major Revision Number** This 8-bit field indicates the major revision number. Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major revisions do not change the overall structure. NOTE Major Revision starts at 0x01and may only be revised by JEDEC.
7:0	**SFDP Minor Revision Number** This 8-bit field indicates the minor revision number. Minor revisions are changes that add parameters in existing Reserved locations, or clarifications to existing fields. Minor revisions do NOT change overall structure of SFDP. NOTE Minor Revision starts at 0x00 and may only be revised by JEDEC.

6.3 Parameter Headers

Identifies the size, location, revision, and ownership of their associated parameter tables. Parameter table ownership will be either JEDEC (via this document) or an individual vendor (via vendor specific documentation).

Multiple parameter headers can be specified with each parameter header being 2 DWORDs (64-bits). The first parameter header is mandatory, defined by JEDEC, and starts at byte offset 0x08. The total number of parameter headers is specified in the NPH field of the SFDP header (see 6.2.3). All subsequent parameter headers need to be contiguous and may be specified by JEDEC or by vendors using the same structure (as shown in 6.1).

6.3 Parameter Headers (cont'd)

6.3.1 Parameter Header: 1st DWORD

Bits	Description
31:24	**Parameter Table Length** This field specifies how many DWORDs are in the Parameter table. Note: This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	**Parameter Table Major Revision Number** This 8-bit field indicates the major revision number. Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Note: Major Revision starts at 0x01. The JEDEC specified Major Revision can only be modified by JEDEC. The vendor specified Major Revision can only be modified by the same vendor.
15:8	**Parameter Table Minor Revision Number** This 8-bit field indicates the minor revision number. Minor revisions are changes that add parameters in existing Reserved locations, or clarifications. Minor revisions do NOT change overall structure of SFDP. Note: Minor Revision starts at 0x00. The JEDEC specified Minor Revision can only be modified by JEDEC. The vendor specified Minor Revision can only be modified by the same vendor.
7:0	**ID Number:** If this field is set to 0x00, it indicates a JEDEC specified header. For vendor specified headers, this field must be set to the vendor's Manufacturer ID.

6.3.2 Parameter Header: 2nd DWORD

Bits	Description
31:24	**Unused** Contains 0xFF and can never be changed.
23:0	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter Table in the SFDP structure. The address must be DWORD-aligned.

6.3 Parameter Headers (cont'd)

6.3.3 Example of an SFDP Header

Figure 5 shows an example of an SFDP Header with SFDP Revision 1.0, one Parameter Header, Parameter Table length of 9 DWORDs, 1st Parameter Header Revision 1.0, JEDEC ID of 0x00, and the Parameter Table Pointer pointing to location 0x000010.

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	0x50	0x44	0x46	0x53	< [3:0]
	0xFF	0x00	0x01	0x00	< [7:4]
1st Parameter Header	0x09	0x01	0x00	0x00	< [B:8]
	0xFF	0x00	0x00	0x10	< [F:C]

Figure 5 — Example of an SFDP Header

6.4 JEDEC Flash Parameter Tables

Parameter tables contain coded information describing the features and capabilities of the serial flash. The first parameter table as defined by JEDEC is mandatory and its starting address is specified by the PTP field of the 1st Parameter Header. The length of this table is nine DWORDs. This table identifies some of the basic features of flash memory devices.

Table 1 — JEDEC Flash Parameters: 1st DWORD

Bits	Description
31:23	**Unused** Contains 0xFF and can never be changed.
22	**Supports (1-1-4) Fast Read** Device supports single input opcode & address and quad output data Fast Read. 0: (1-1-4) Fast Read NOT supported. 1: (1-1-4) Fast Read supported.
21	**Supports (1-4-4) Fast Read** Device supports single input opcode, quad input address, and quad output data Fast Read. 0: (1-4-4) Fast Read NOT supported. 1: (1-4-4) Fast Read supported.
20	**Supports (1-2-2) Fast Read** Device supports single input opcode, dual input address, and dual output data Fast Read. 0: (1-2-2) Fast Read NOT supported. 1: (1-2-2) Fast Read supported.
19	**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. 0: DTR NOT supported 1: DTR Clocking supported
18:17	**Address Bytes** Number of bytes used in addressing flash array read, write and erase: 00: 3-Byte only addressing 01: 3- or 4-Byte addressing (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10: 4-Byte only addressing 11: Reserved NOTE All flash devices under 128 megabits in size should use 00b for this value for 24 bit addressing. This field refers to the number of address bits/bytes that are clocked in for any instruction requiring an address in the flash array. This field does not pertain to SFDP Header or Table accesses; all SFDP accesses use 3-byte addressing. Examples: Read, Fast Read, Write, 4 kilobyte Erase.

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 1 — JEDEC Flash Parameters: 1st DWORD (cont'd)

Bits	Description
16	**Supports (1-1-2) Fast Read** Device supports single input opcode & address and dual output data Fast Read with 8 bits of wait states. 0: (1-1-2) Fast Read NOT supported. 1: (1-1-2) Fast Read supported.
15:8	**4 Kilobyte Erase Opcode** **Note:** If 4 kilobyte erase is not supported, then enter 0xFF.
7:5	**Unused** Contains 111b and can never be changed.
4	**Write Enable Opcode Select for Writing to Volatile Status Register** 0: 0x50 is the Opcode to enable a status register write when bit 3 is set to 1. 1: 0x06 is the Opcode to enable a status register write when bit 3 is set to 1. NOTE If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.
3	**Write Enable Instruction Required for Writing to Volatile Status Register** 0: Target flash has nonvolatile status bit and does not require status register to be written on every power on to allow writes and erases. 1: Target flash requires a 0x00 to be written to the status register in order to allow writes and erases. NOTE If target flash register is nonvolatile, then bits 3 and 4 must be set to 00b.
2	**Write Granularity** 0: 1 Byte – Use this setting for single byte programmable devices or buffer programmable devices when the buffer is less than 64 bytes (32 Words). 1: Use this setting for buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger.
1:0	**Block/Sector Erase Sizes** Identifies the erase granularity for all Flash Components. 00: Reserved 01: 4 kilobyte Erase 10: Reserved 11: Use this setting only if the 4 kilobyte erase is unavailable.

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 2 — JEDEC Flash Parameter: 2nd DWORD

Bits	Description
31:0	**Flash Memory Density** For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. **Example** 0x00FFFFFF = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be >= 32). **Example** 0x80000021 = 2^33 = 8 gigabits

Table 3 — JEDEC Flash Parameters: 3rd DWORD

Bits	Description
31:24	**(1-1-4) Fast Read Opcode** Opcode for single input opcode & address and quad output data Fast Read.
23:21	**(1-1-4) Fast Read Number of Mode Bits** This field will be 000b if Mode Bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example** If 4 mode bits are needed with a single input address phase instruction, this field would be 100b.
20:16	**(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example** If 8 bits are needed with a single input address phase instruction, this field would be 01000b.
15:8	**(1-4-4) Fast Read Opcode** Opcode for single input opcode, quad input address, and quad output data Fast Read.
7:5	**Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example** If 8 mode bits are needed with a quad input address phase instruction, this field would be 010b.
4:0	**(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example** If 16 bits are needed with a quad input address phase instruction, this field would be 00100b.

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 4 — JEDEC Flash Parameters: 4th DWORD

Bits	Description
31:24	**(1-2-2) Fast Read Opcode** Opcode for single input opcode, dual input address, and dual output data Fast Read.
23:21	**(1-2-2) Fast Read Number of Mode Bits** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example** If 8 mode bits are needed with a dual input address phase instruction, this field would be 100b.
20:16	**(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example** If 8 bits are needed with a dual input address phase instruction, this field would be 00100b.
15:8	**(1-1-2) Fast Read Opcode** Opcode for single input opcode& address and dual output data Fast Read. Note: The industry standard is 0x3B
7:5	**(1-1-2) Fast Read Number of Mode Bits** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. **Example** If 4 mode bits are needed with a single input address phase instruction, this field would be 100b.
4:0	**(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field should be programmed with 01000b for 8 clocks of dummy cycle. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) NOTE For legacy reasons, if dummy clocks for this opcode is not 01000b, then bit 16 of Flash Basic Properties offset 0 (Supports (1-1-2) Fast Read) must NOT be set to '1'.

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 5 — JEDEC Flash Parameters: 5th DWORD

Bits	Description
31:5	Reserved. These bits default to all 1's
4	**Supports (4-4-4) Fast Read** Device supports Quad input opcode & address and quad output data Fast Read. 0: (4-4-4) Fast Read NOT supported. 1: (4-4-4) Fast Read supported.
3:1	Reserved. These bits default to all 1's
0	**Supports (2-2-2) Fast Read** Device supports dual input opcode& address and dual output data Fast Read. 0: (2-2-2) Fast Read NOT supported. 1: (2-2-2) Fast Read supported.

Table 6 — JEDEC Flash Parameters: 6th DWORD

Bits	Description
31:24	**(2-2-2) Fast Read Opcode** Opcode for dual input opcode& address and dual output data Fast Read.
23:21	**(2-2-2) Fast Read Number of Mode Bits** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example** If 4 mode bits are needed with a (2-2-2) Fast Read instruction, this field would be 010b.
20:16	**(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example** If 8 bits are needed with a (2-2-2) Fast Read instruction, this field would be 00100b.
15:0	Reserved. These bits default to all 1's

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 7 — JEDEC Flash Parameters: 7th DWORD

Bits	Description
31:24	**(4-4-4) Fast Read Opcode** Opcode for quad input opcode/address, quad output data Fast Read.
23:21	**(4-4-4) Fast Read Number of Mode Bits** This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The master drives the bus during "mode bits" cycles; the master tri-states the bus during "dummy" cycles. **Example** If 8 mode bits are needed with a (4-4-4) Fast Read phase instruction, this field would be 010b.
20:16	**(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) **Example** If 16 bits are needed with a (4-4-4) Fast Read phase instruction, this field would be 00100b.
15:0	Reserved. These bits default to all 1's

Table 8 — JEDEC Flash Parameters: 8th DWORD

Bits	Description
31:24	**Sector Type 2 Opcode** Opcode used to erase the number of bytes specified by Sector Type 2 Size (bits 23-16).
23:16	**Sector Type 2 Size:** This field will be 0x00 if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example** If the sector size is 32 kilobytes, this field would 0x0F.
15:8	**Sector Type 1 Opcode** Opcode used to erase the number of bytes specified by Sector Type 1 Size (bits 7-0).
7:0	**Sector Type 1 Size** NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example** If the sector size is 4 kilobytes, this field would 0x0C.

6.4 JEDEC Flash Parameter Tables (cont'd)

Table 9 — JEDEC Flash Parameters: 9th DWORD

Bits	Description
31:24	**Sector Type 4 Opcode** Opcode used to erase the number of bytes specified by Sector Type 4 Size (bits 23-16).
23:16	**Sector Type 4 Size** This field will be 0x00 if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example** If the sector size is 256 kilobytes, this field would 0x12.
15:8	**Sector Type 3 Opcode** Opcode used to erase the number of bytes specified by Sector Type 3 Size (bits 7-0).
7:0	**Sector Type 3 Size** This field will be 0x00 if this sector type does not exist. NOTE This field specifies 'N' and is used to calculate sector/block size = 2^N bytes **Example** If the sector size is 64 kilobytes, this field would 0x10.

7 Rules for Header and Table Additions and Modifications

- Additional headers and parameter tables can be added by vendors without JEDEC approval.
- The first four DWORDs of the 6.4 JEDEC Flash Parameters Table can never be modified.
- New headers must be built using exactly two DWORDs and they must immediately follow the existing header(s).
- Minimum parameter table size is one DWORD. The maximum parameter table size is not specified.
- Parameter tables may be located anywhere in the SFDP space. They do not need to immediately follow the parameter headers.
- Overlapping parameter tables are permitted.

8 Legacy Compatibility

Prior to the release of this document, Intel published SFDP guidelines with a four DWORD parameter table. The first four DWORDs of the JEDEC Parameter Table are identical to the table in Intel's guidelines. Devices in production prior to the release of JESD216 might only contain these four DWORDs.

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