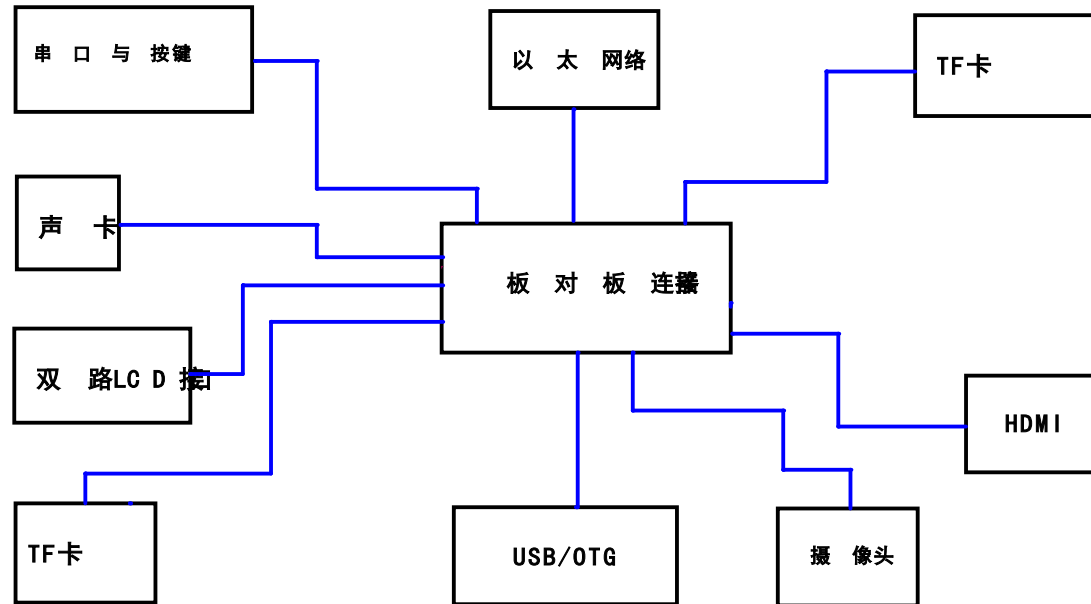
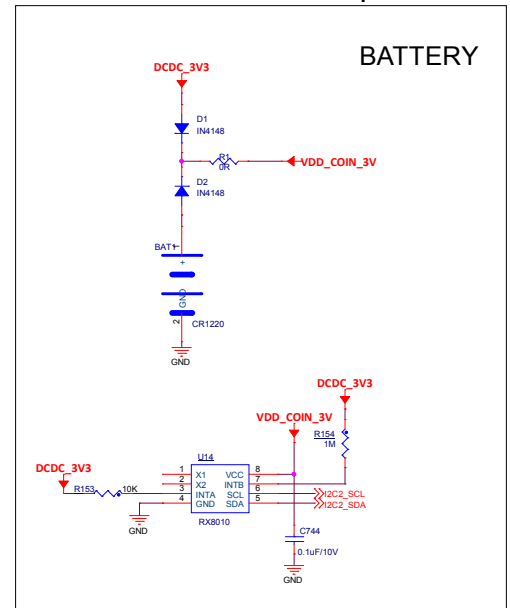


Table of Contents	Part Reference	Details of Revision

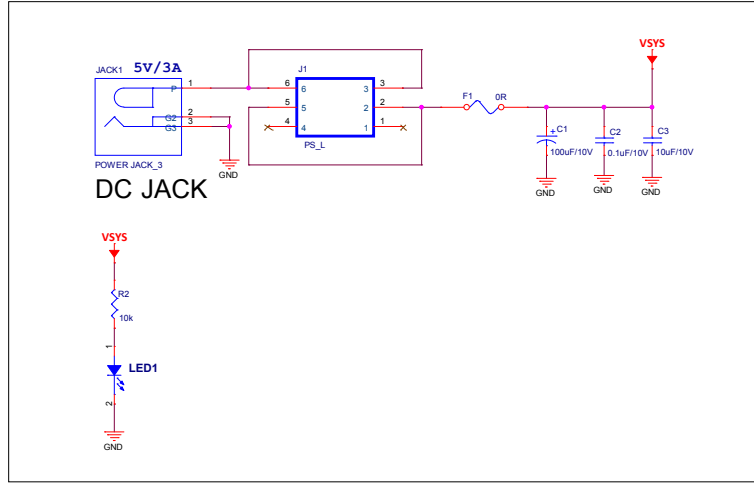
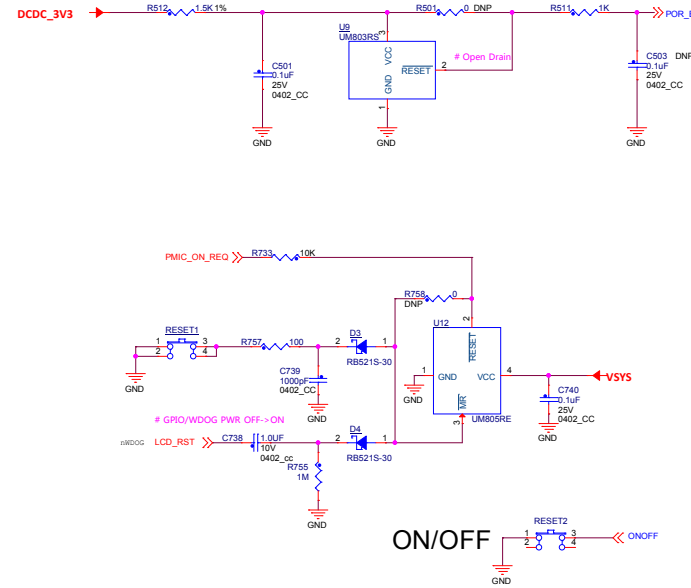
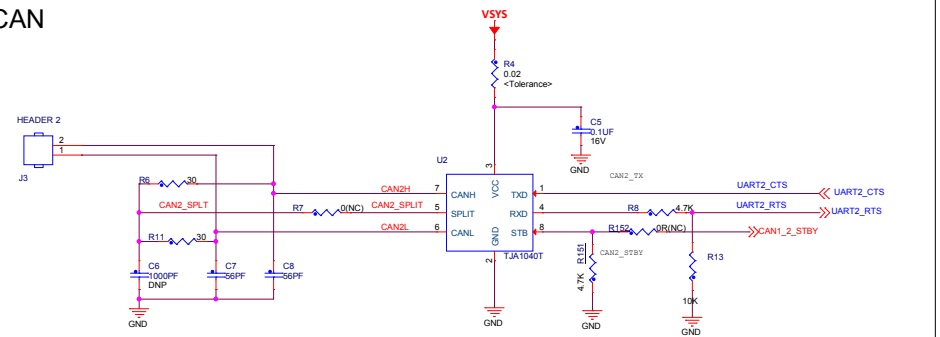


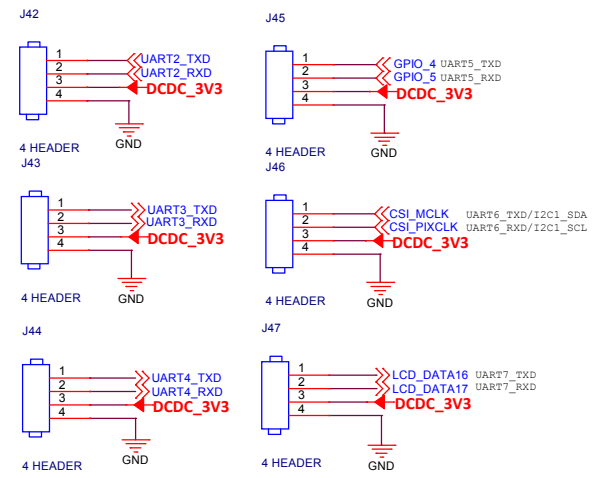
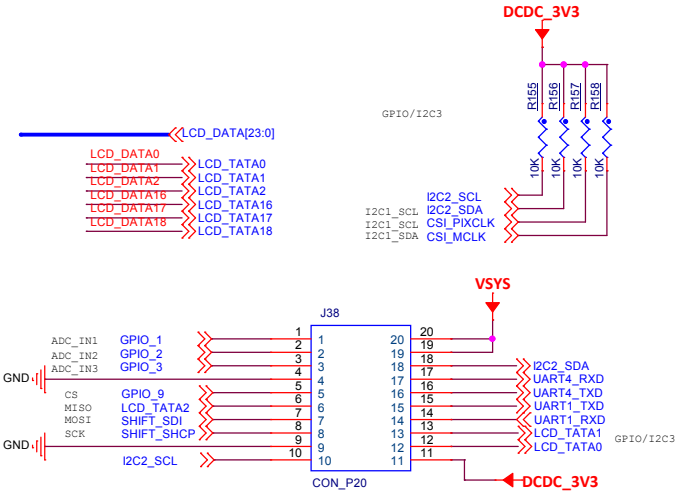
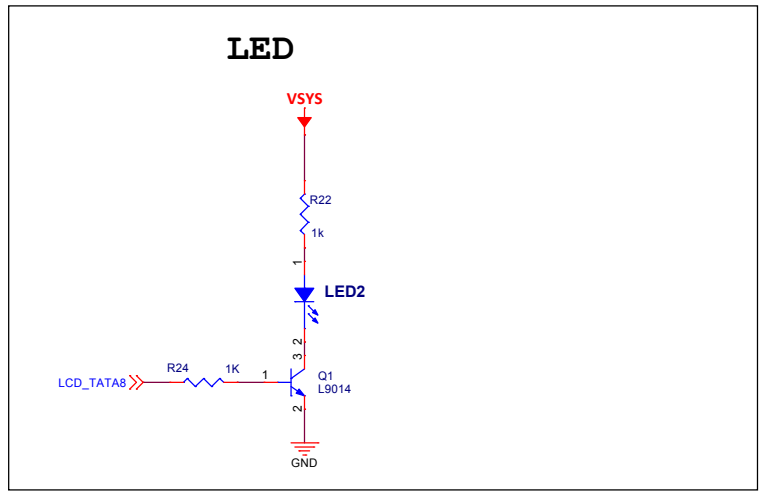
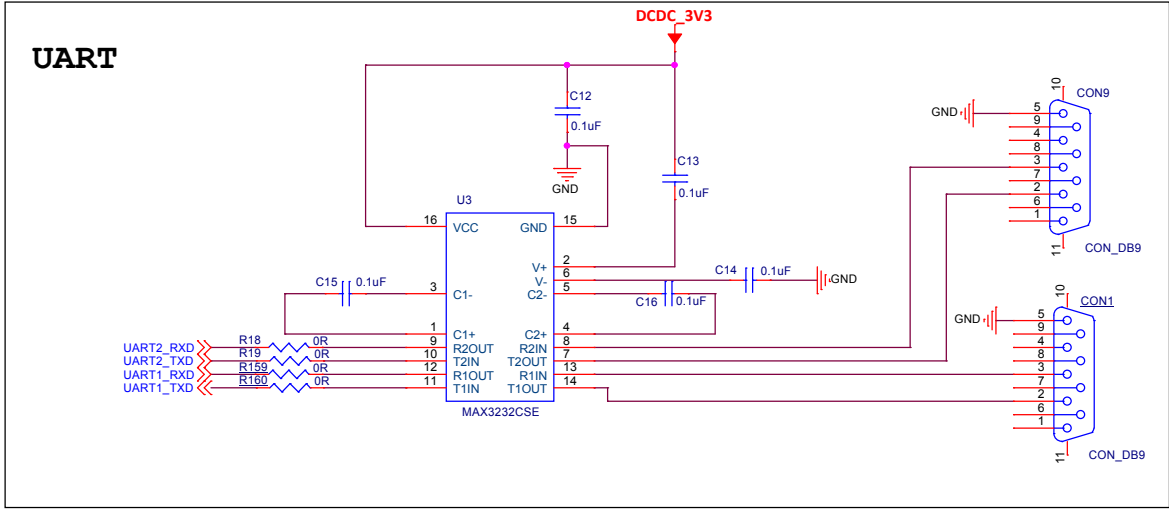


Mounting holes Boards



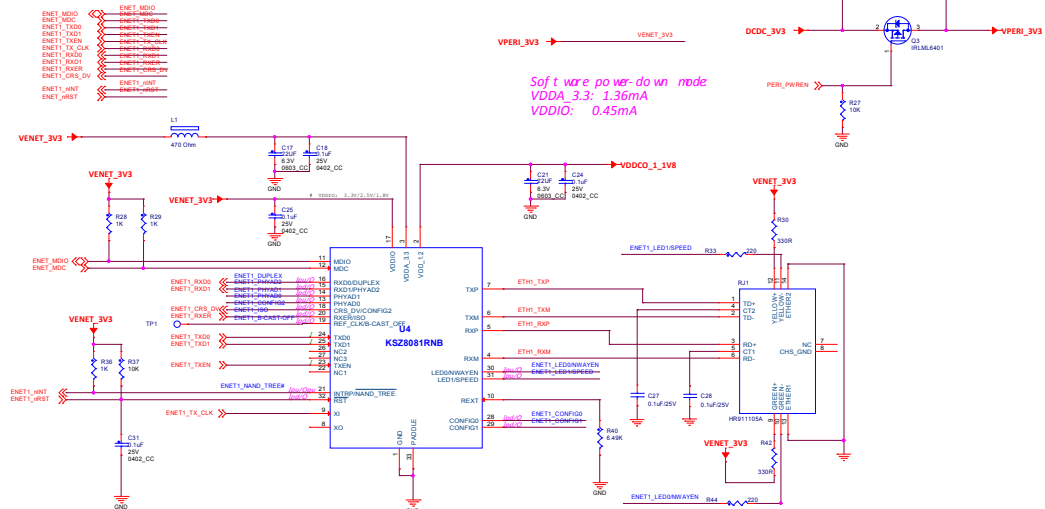
CAN



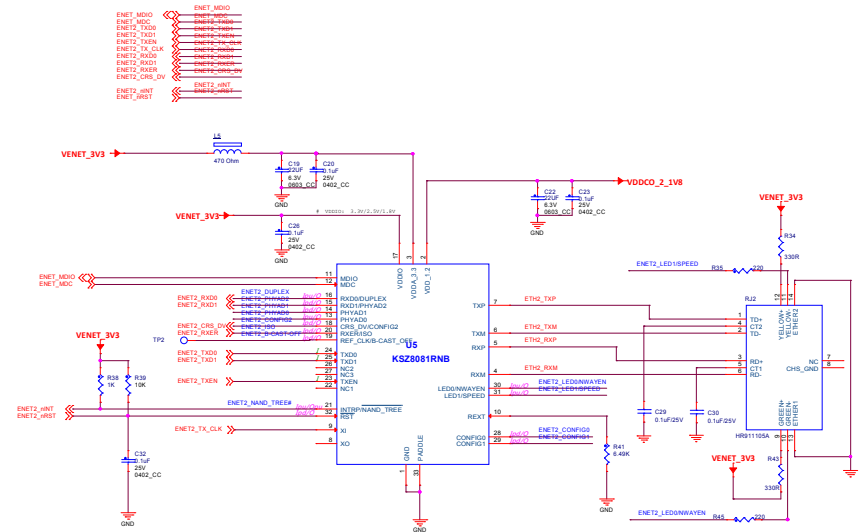


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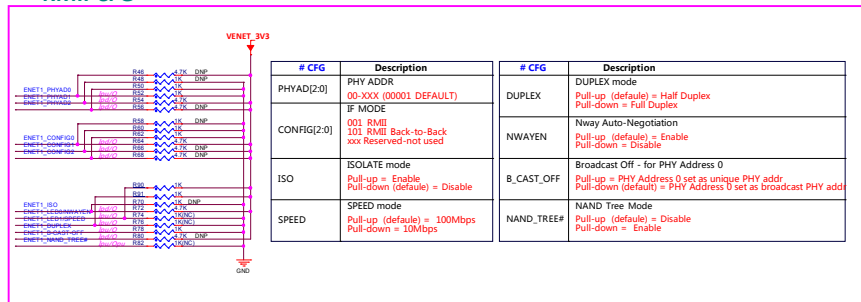
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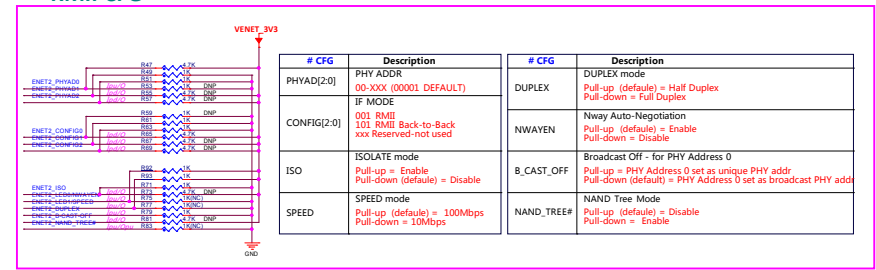
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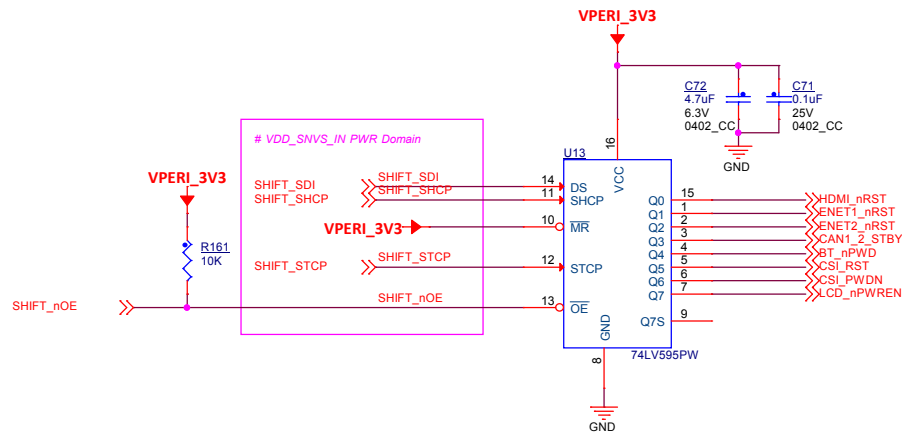
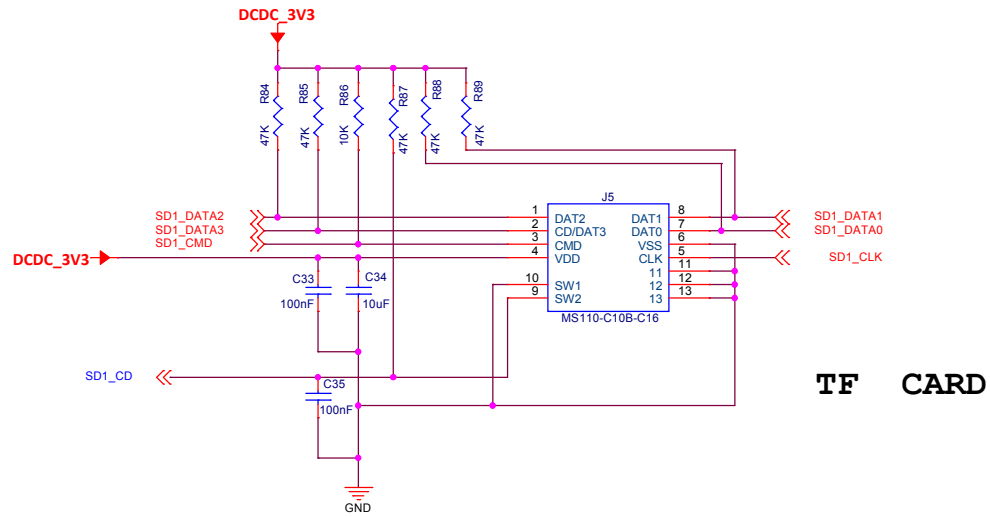


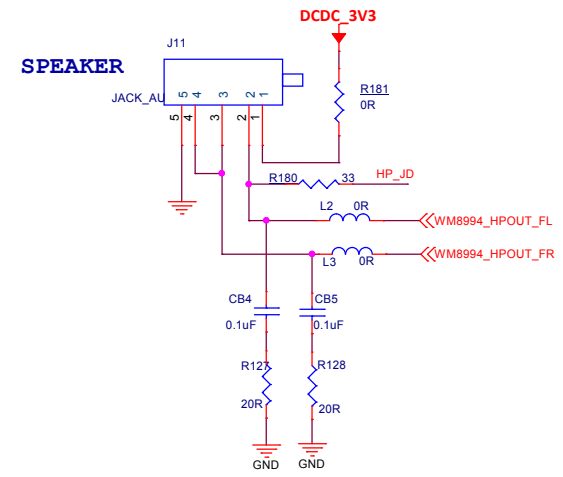
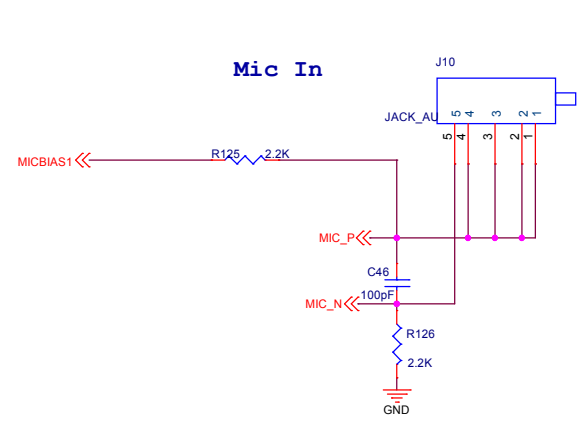
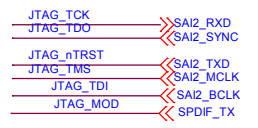
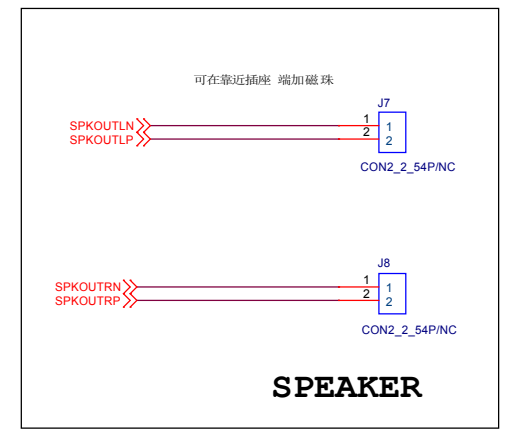
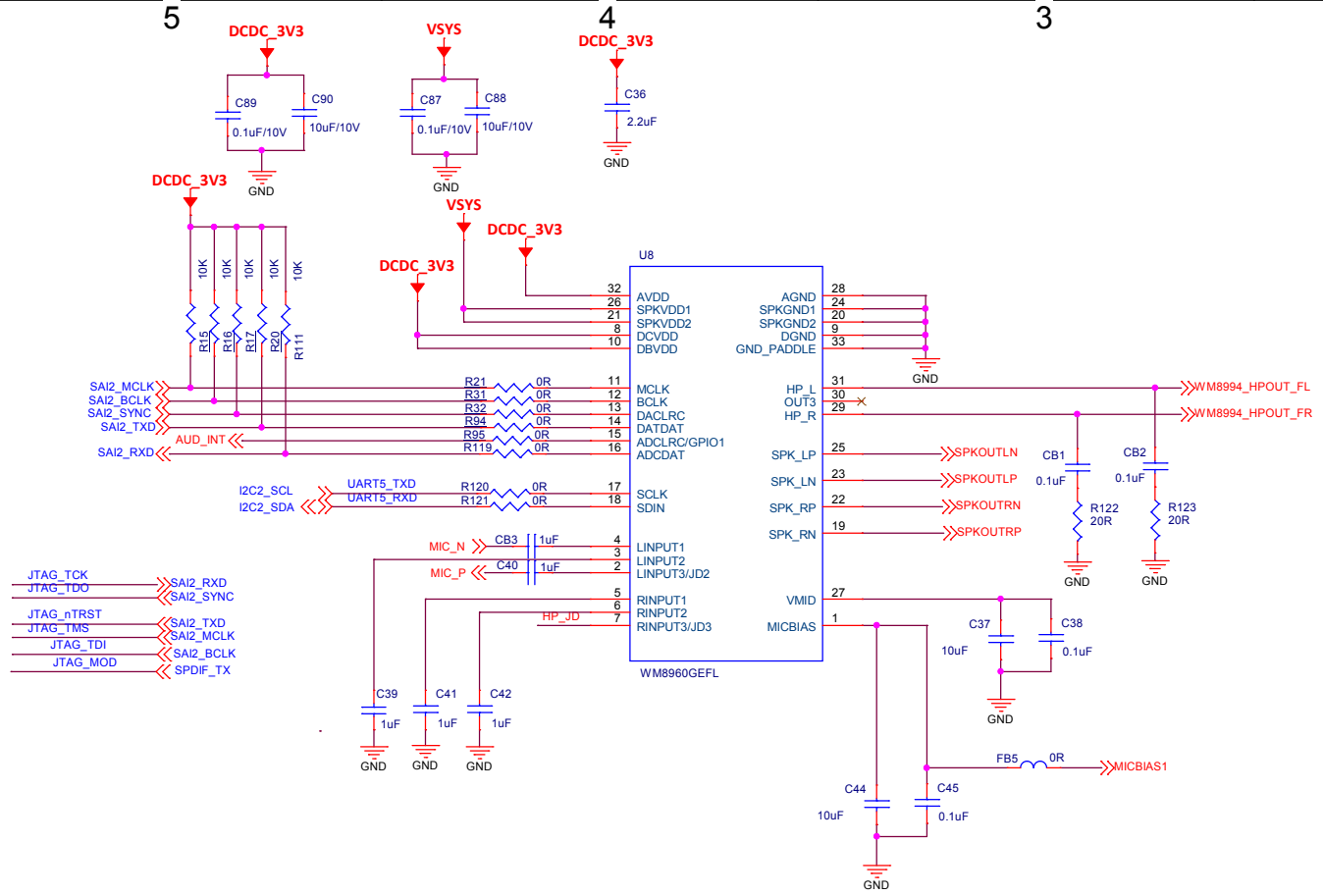
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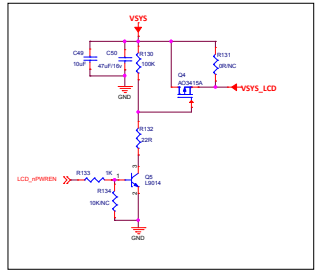
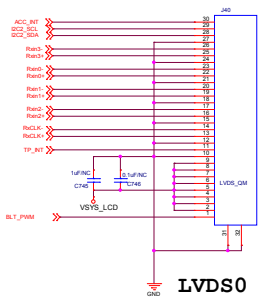
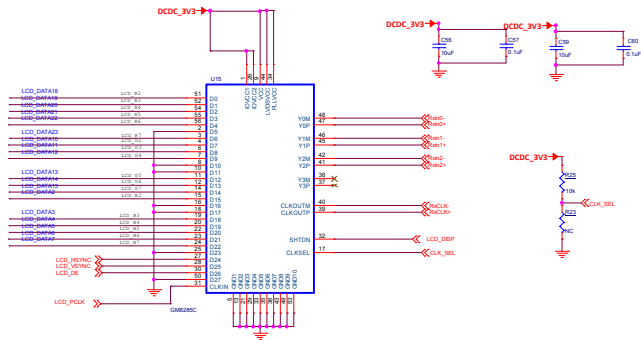
RMII CFG



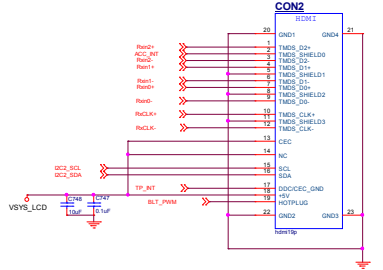
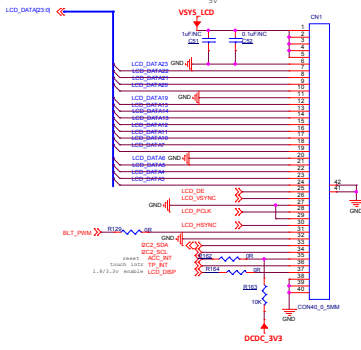




RGB TO LVDS



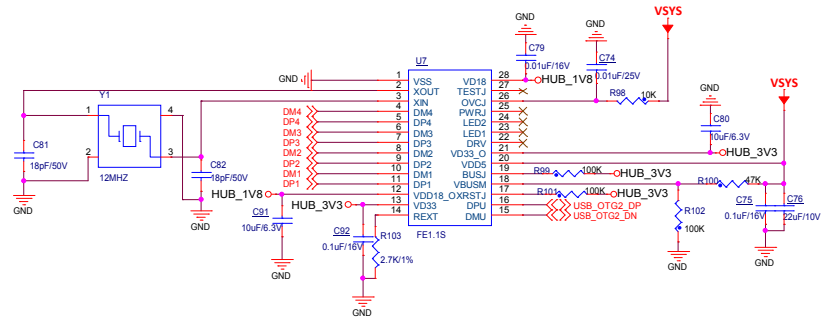
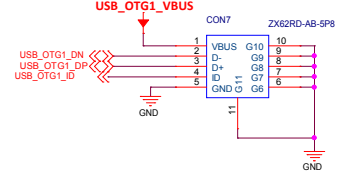
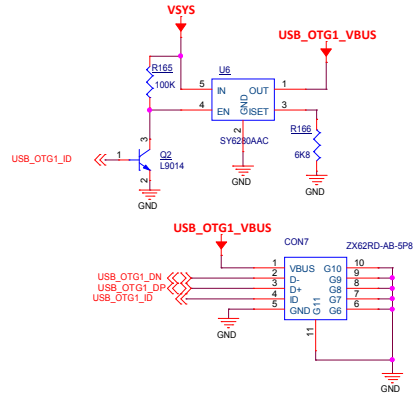
4.3 LCD RGB Interface



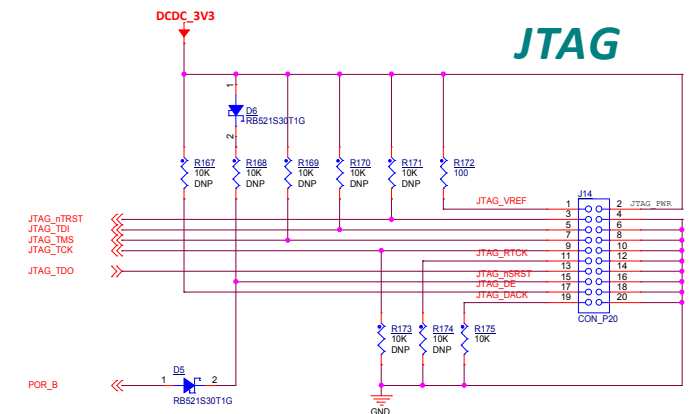
USB HOST/OTG

- USB_OTG1_DN <-> USB_OTG1_DN
- USB_OTG1_DP <-> USB_OTG1_DP
- USB_OTG2_DN <-> USB_OTG2_DN
- USB_OTG2_DP <-> USB_OTG2_DP

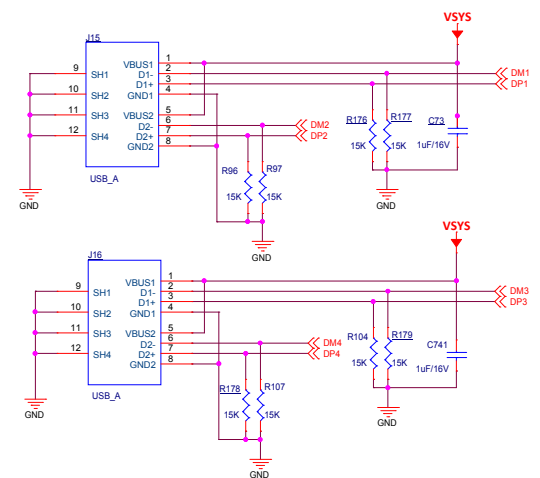
- USB_OTG1_PWR <-> USB_OTG1_PWR
- USB_OTG2_PWR <-> USB_OTG2_PWR
- USB_OTG1_ID <-> USB_OTG1_ID
- USB_OTG1_OC <-> USB_OTG1_OC
- USB_OTG2_OC <-> USB_OTG2_OC

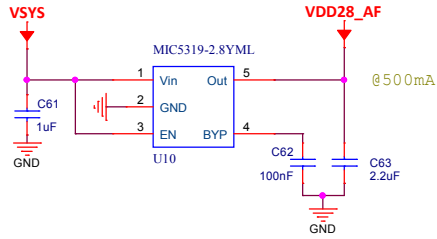


JTAG

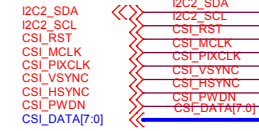


USB HOST

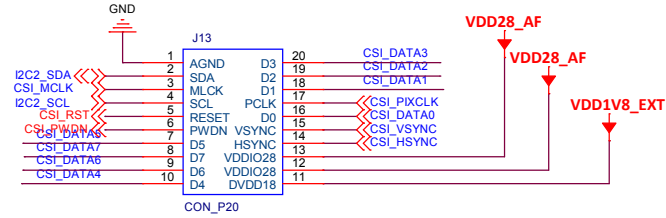
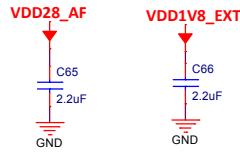




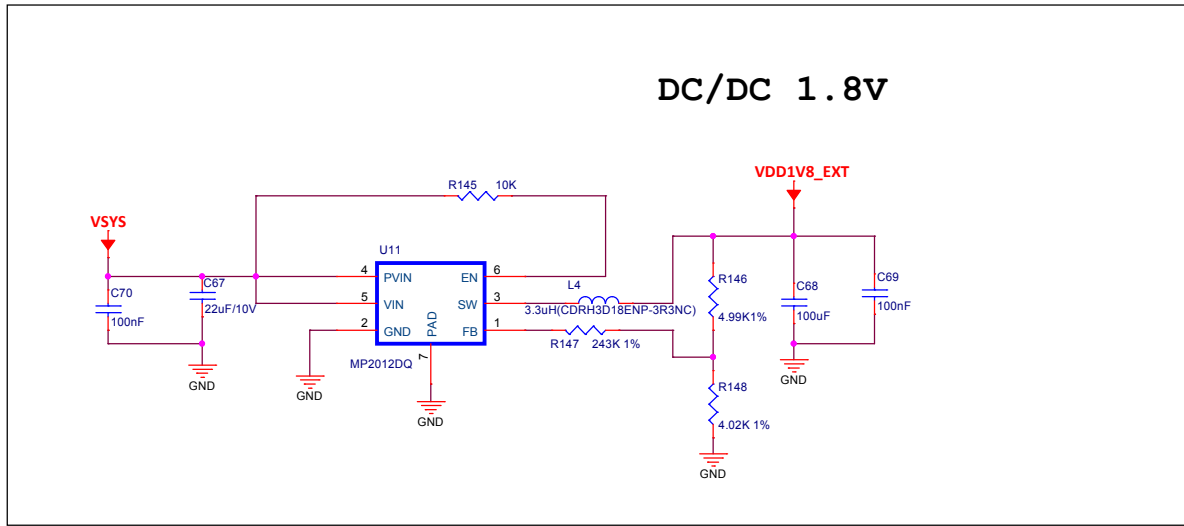
Camera / SIM



CAMERA Connector AVIN Connector



DC/DC 1.8V



FUSE MAP

<Default: QSPI BOOT>
0/1 0/1 0/1 1 0 0 0 0

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved		DDRSMP: "000": Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDHC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_RST pad (USDMC2 & 4 only)	SD Loopback Clock Source Sel for SDR50 and SDR104 only 0 - through SD pad 1 - direct	
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDMC_RST pad (USDMC2 & 4 only)	SD Loopback Clock Source Sel for SDR50 and SDR104 only 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256	Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved	Nand Row Address Bytes: 00 - 3 01 - 2 10 - 4 11 - 5			

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HPMS: Half Speed Phase Select (on TBD) - 1 TBD	HSCLK: Half Speed Delay Select (on TBD) - 1 TBD	HPMS: Full Speed Phase Select (on TBD) - 1 TBD	HSCLK: Full Speed Delay Select (on TBD) - 1 TBD	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Mixing Scheme: 00 - A/D16 01 - A+D8 10 - A+D4 11 - Reserved	OneWord Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Reserved	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibrat i on & sep '00' - 1 TBD	Bus Width: 0 - 1-bit 1 - 4-bit TBD	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD2 VOLTAGE SELECTION 0 - 1.8V 1 - 1.9V	Reserved	Reserved	Reserved
MMC/eMMC	Bus Width: 000 - 4-bit 001 - 4-bit 010 - 4-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Ehc - reserved	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 1.8V 1 - 1.9V	Reserved	Reserved	Reserved	Reserved
NAND	Toggle Mode (33MHz Preamble Delay, Read Latency) '00' - 16 GPMCLK cycles '01' - 3 GPMCLK cycles '10' - 2 GPMCLK cycles '11' - 3 GPMCLK cycles '100' - 4 GPMCLK cycles '101' - 5 GPMCLK cycles '110' - 6 GPMCLK cycles '111' - 7 GPMCLK cycles	BOOT_SEARCH_COUNT: 00 - 2 01 - 3 10 - 4 11 - 8	Boot Frequencies (ARM/DMA) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Boot Time 0 - 2ms 1 - 2.5ms (LBA Next)	Reserved	Reserved	Reserved	Reserved

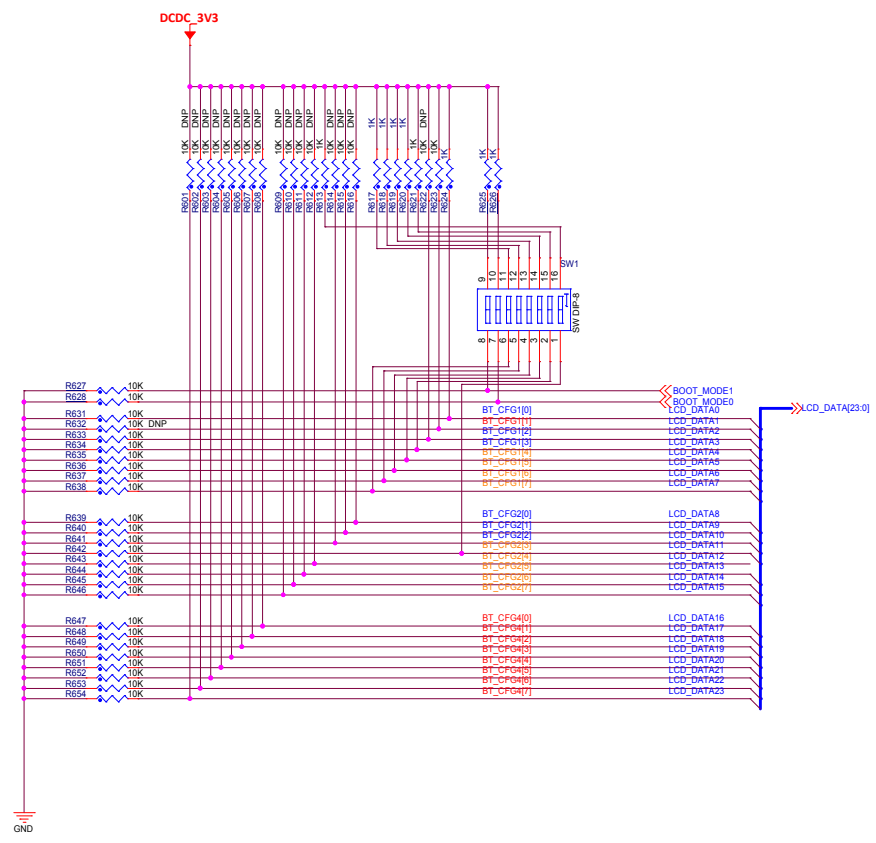
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infi nit-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Reserved	Reserved	Reserved	Reserved
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Ref) ect ed n SB M3	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 confi g opti on)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x470	DLL Override: 0 - DLL Stave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDRAM Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	MMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDMC_PAD_PULL_DOWN 0 - no sct i on 1 - pull-down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDMC_IOMUX_SION_BIT_ENA 0 - Disable 1 - Enable	ALBSDMC_IOMUX_SRE_Enable 0 - Disable 1 - Enable
0x470	USDMC_CMD_DE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR - Bus) '00' - LPB Disable '01' - 1 GPO (def freq) '10' - Div by 2 '11' - Div by 4	BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)				
0x470	Override NAND Pad Set 1 mg (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

NAND MT29F32G08CBACA

1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= (1024K + 56K) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17.280Mb
1 LUN = 17.280Mb x 2 planes
= 34.560Mb

Boot Configuratio

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



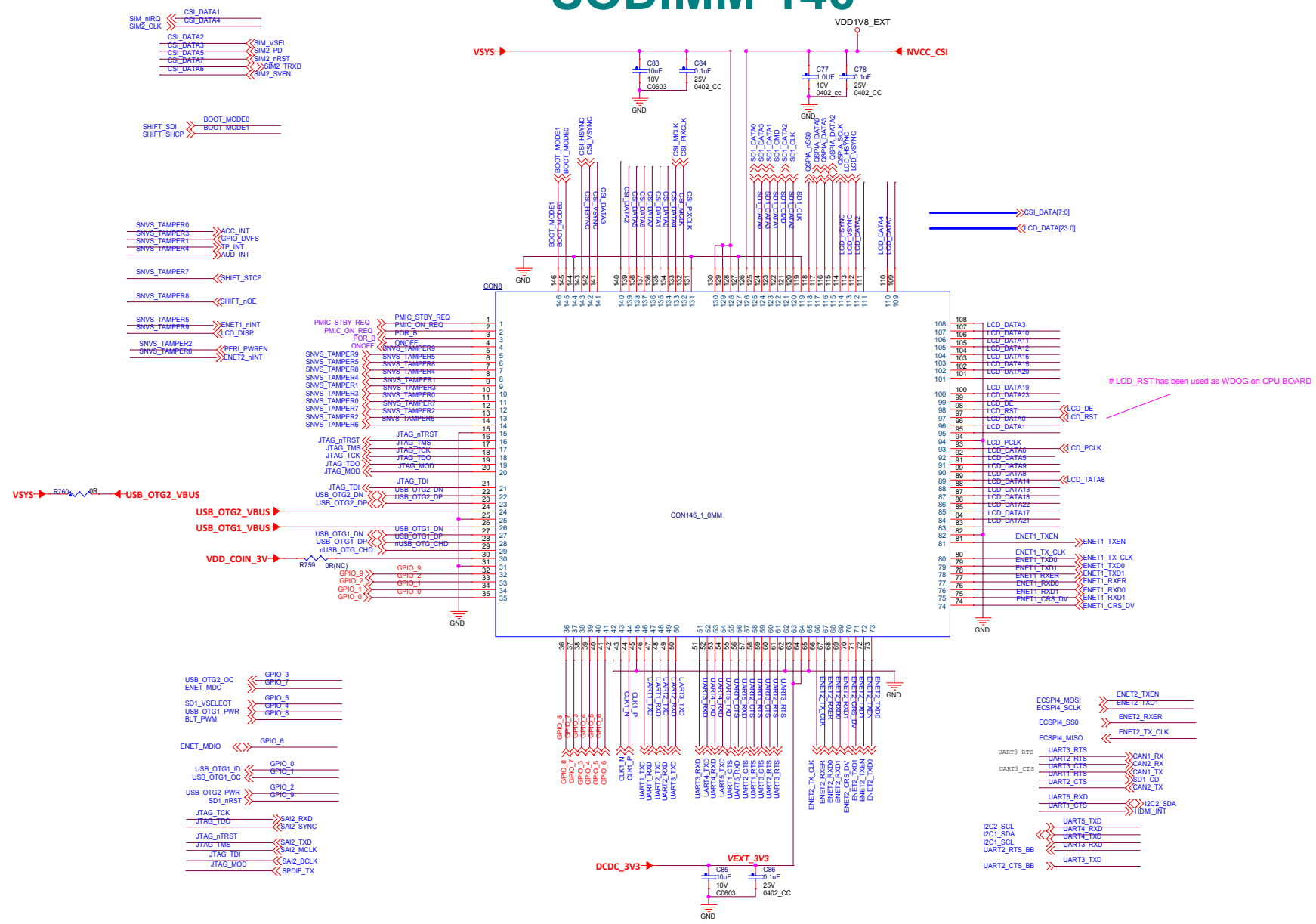
freescale Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8588

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Drawn by: DRAWN_BY
Page Title: BOOT CFG
Approved: APPROVER
Size C
Document Number: SCH-28617 PDF: SPF-28617
Rev C1
Date: Wednesday, November 20, 2019
Sheet 9 of 13

SODIMM 146



Title		
BOARD CONNECTOR		
Size	Document Number	Rev
C		V1.0
Date:	Wednesday, June 27, 2018	Sheet 11 of 11