MCIMX6UL-CORE

Schematics CoreBoard

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Revision History

Rev. Code	Date	Description
V1.0	2018-02-28	Revision 1.0 release
V1.1	2018-04-14	1.Delete R405,R709,R731. 2.Delete power VLDO_3V3,NVCC_SD. 3.Add NANDFLASH.

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Title: Cover

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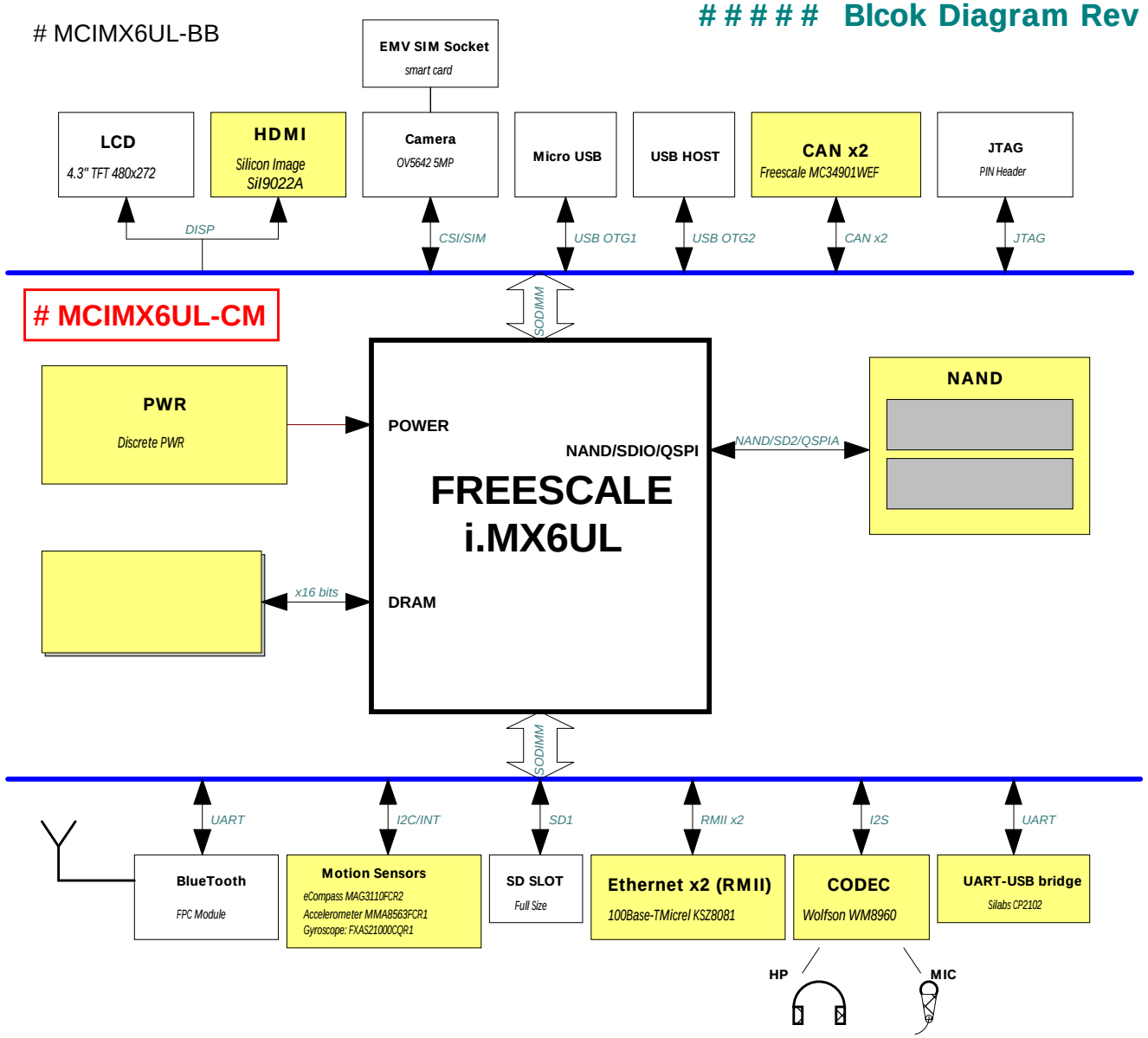
i.MX6UL EVK Block Diagram

Blcok Diagram Rev 1.0

MPN: MCIMX6UL-BB Agile No: 28616
MPN: MCIMX6UL-CM Agile No: 28617



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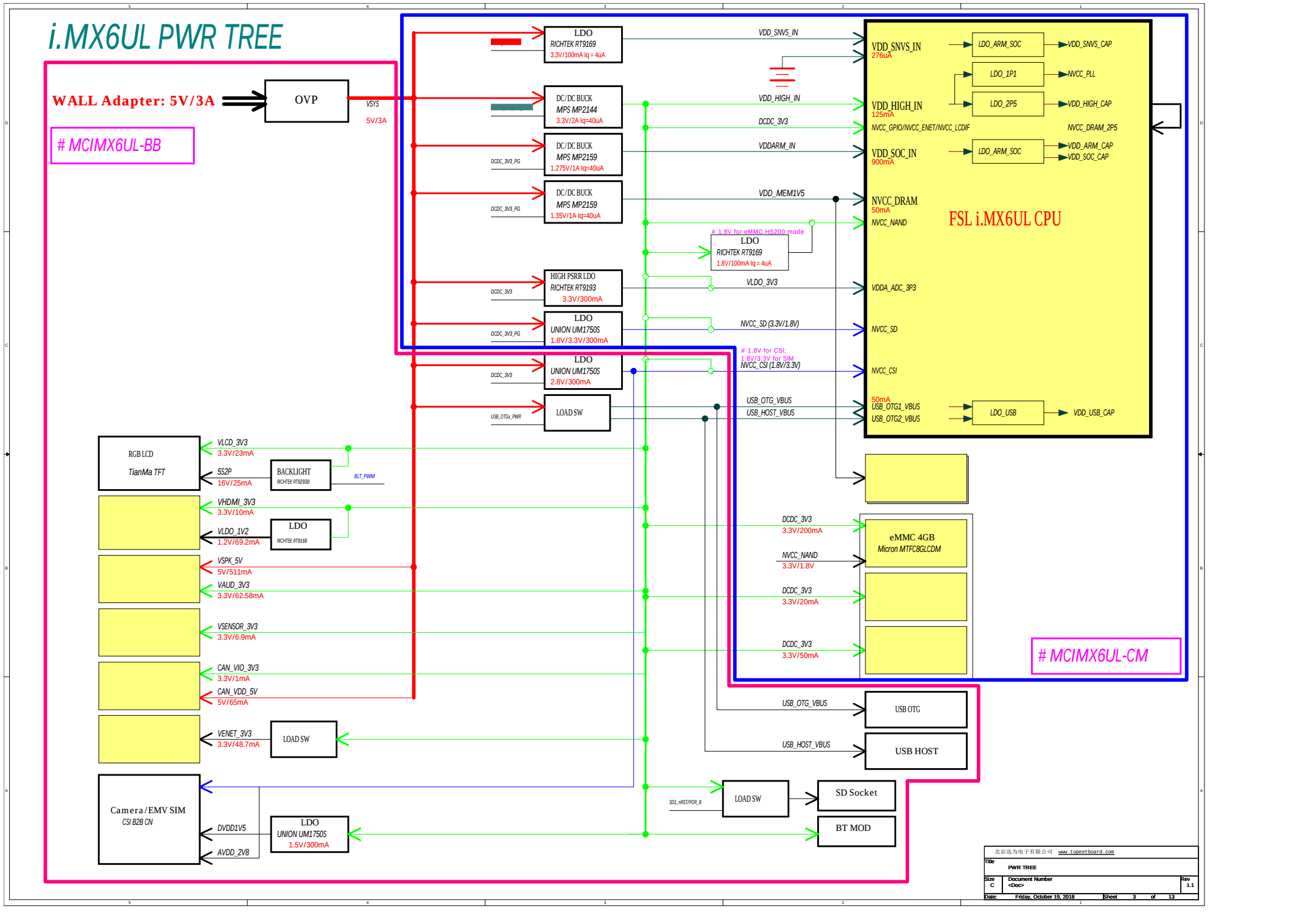
i.MX6UL PWR TREE
WALL Adapter: 5V/3A
OVP
VSYS
5V/3A
MCIMX6UL-BB
LDO
RICHTEK RT9169
3.3V/100mA Iq = 4uA
VDD_SNVS_IN
DC/DC BUCK
MPS MP2144
3.3V/2A Iq=40uA
VDD_HIGH_IN
DCDC_3V3
DC/DC BUCK
MPS MP2159
1.275V/1A Iq=40uA
VDDARM_IN
DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.35V/1A Iq=40uA
VDD_MEM1V5
DCDC_3V3_PG
1.8V for eMMC HS200 mode
LDO
RICHTEK RT9169
1.8V/100mA Iq = 4uA
HIGH PSRR LDO
RICHTEK RT9193
3.3V/300mA
VLDO_3V3
DCDC_3V3
LDO
UNION UM1750S
1.8V/3.3V/300mA
NVCC_SD (3.3V/1.8V)
DCDC_3V3_PG
1.8V for CSI;
1.8V/3.3V for SIM
LDO
UNION UM1750S
2.8V/300mA
NVCC_CSI (1.8V/3.3V)
DCDC_3V3
LOAD SW
USB_OTG_VBUS
USB_HOST_VBUS
USB_OTGx_PWR
VDD_SNVS_IN
276uA
LDO_ARM_SOC
VDD_SNVS_CAP
LDO_1P1
NVCC_PLL
VDD_HIGH_IN
125mA
LDO_2P5
VDD_HIGH_CAP
NVCC_GPIO/NVCC_ENET/NVCC_LCDIF
NVCC_DRAM_2P5
VDD_SOC_IN
900mA
LDO_ARM_SOC
VDD_ARM_CAP
VDD_SOC_CAP
NVCC_DRAM
50mA
NVCC_NAND
FSL i.MX6UL CPU
VDDA_ADC_3P3
NVCC_SD
NVCC_CSI
50mA
USB_OTG1_VBUS
USB_OTG2_VBUS
LDO_USB
VDD_USB_CAP
RGB LCD
TianMa TFT
VLCD_3V3
3.3V/23mA
5S2P
16V/25mA
BACKLIGHT
RICHTEK RT9293B
BLT_PWM
VHDMI_3V3
3.3V/10mA
VLDO_1V2
1.2V/69.2mA
LDO
RICHTEK RT9169
VSPK_5V
5V/511mA
VAUD_3V3
3.3V/62.58mA
VSENSOR_3V3
3.3V/6.9mA
CAN_VIO_3V3
3.3V/1mA
CAN_VDD_5V
5V/65mA
VENET_3V3
3.3V/48.7mA
LOAD SW
Camera/EMV SIM
CSI B2B CN
DVDD1V5
AVDD_2V8
LDO
UNION UM1750S
1.5V/300mA
DCDC_3V3
3.3V/200mA
eMMC 4GB
Micron MTFC8GLCDM
NVCC_NAND
3.3V/1.8V
DCDC_3V3
3.3V/20mA
DCDC_3V3
3.3V/50mA
MCIMX6UL-CM
USB_OTG_VBUS
USB OTG
USB_HOST_VBUS
USB HOST
SD1_nRST/POR_B
LOAD SW
SD Socket
BT MOD
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Title
PWR TREE
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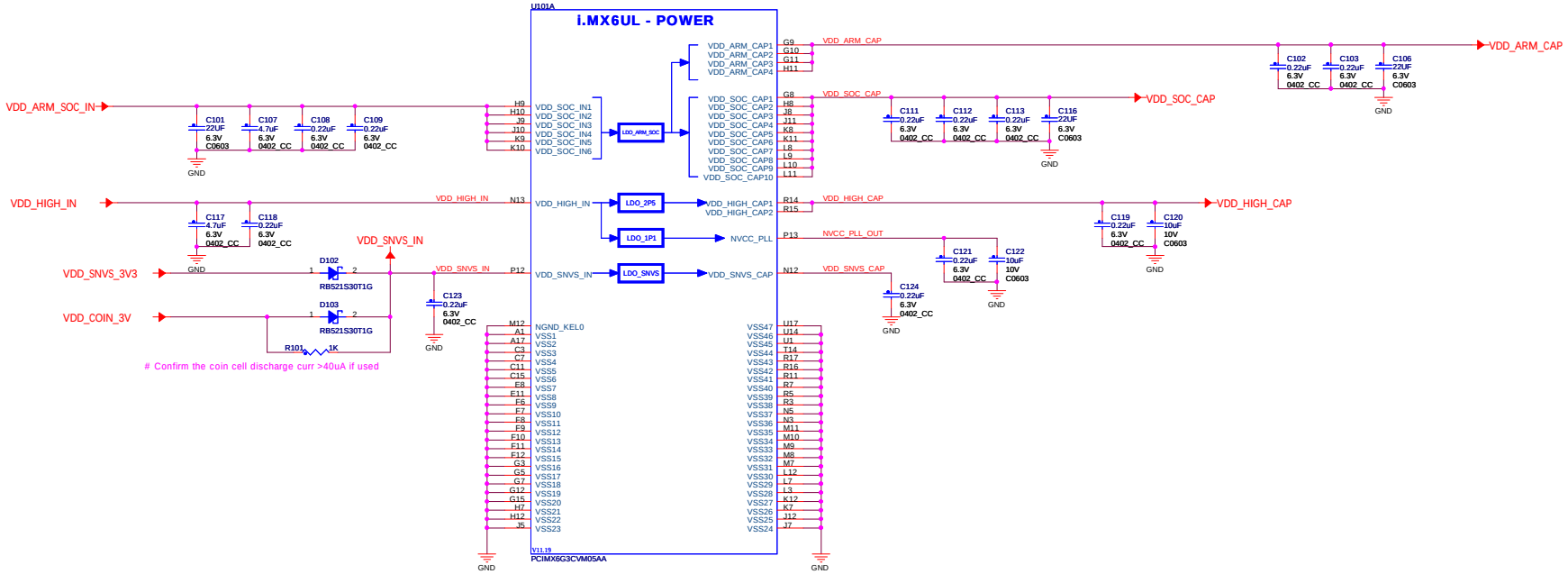
i.MX6UL PWR



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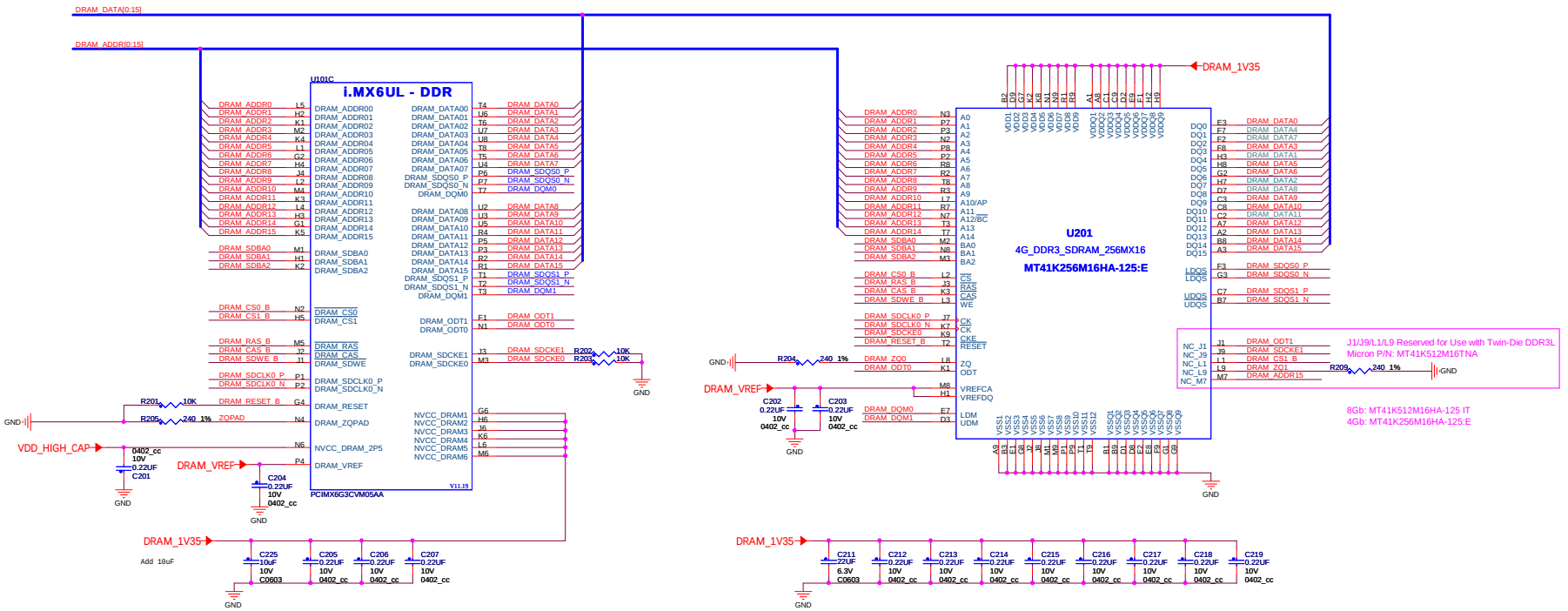
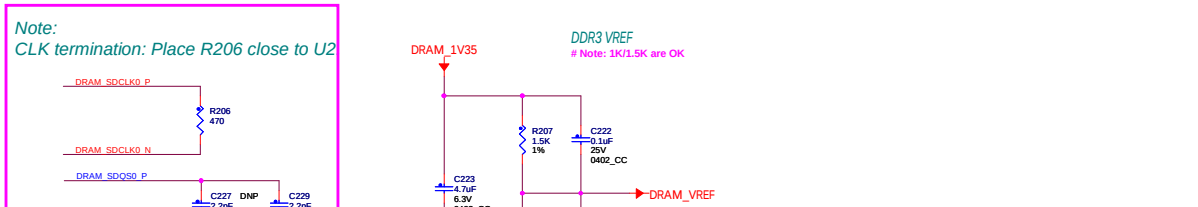
DDR3/LvDDR3





Note:
CLK termination: Place R206 close to U2

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Title: LvDDR3			
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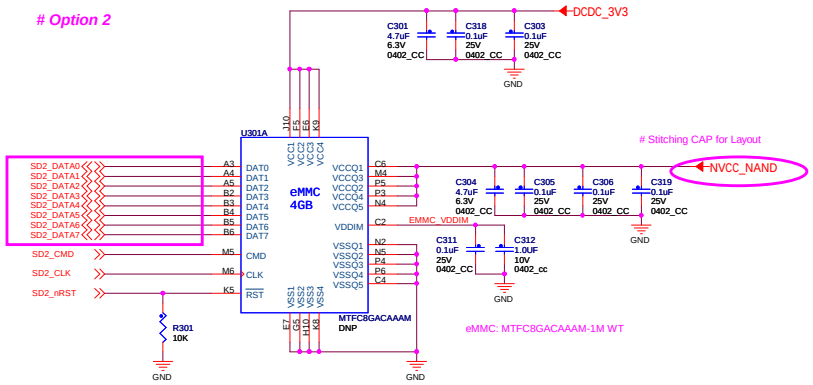
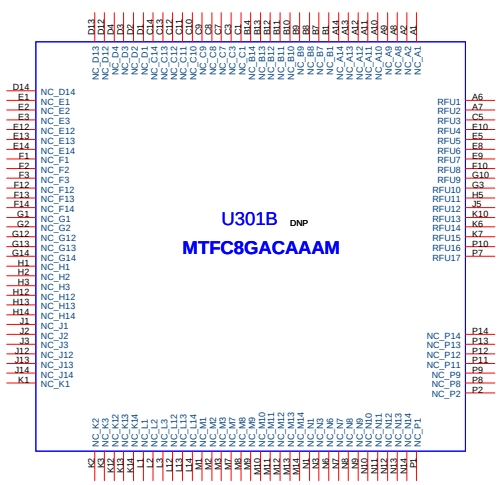
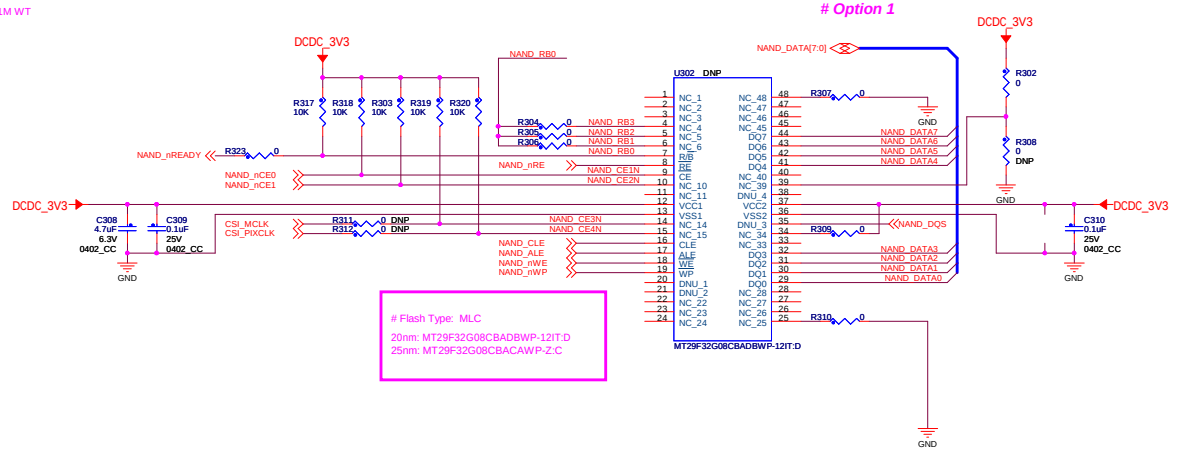
eMMC Storage <4.51>





NAND FLASH



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Title: eMMC/NAND/TF/QSPI		
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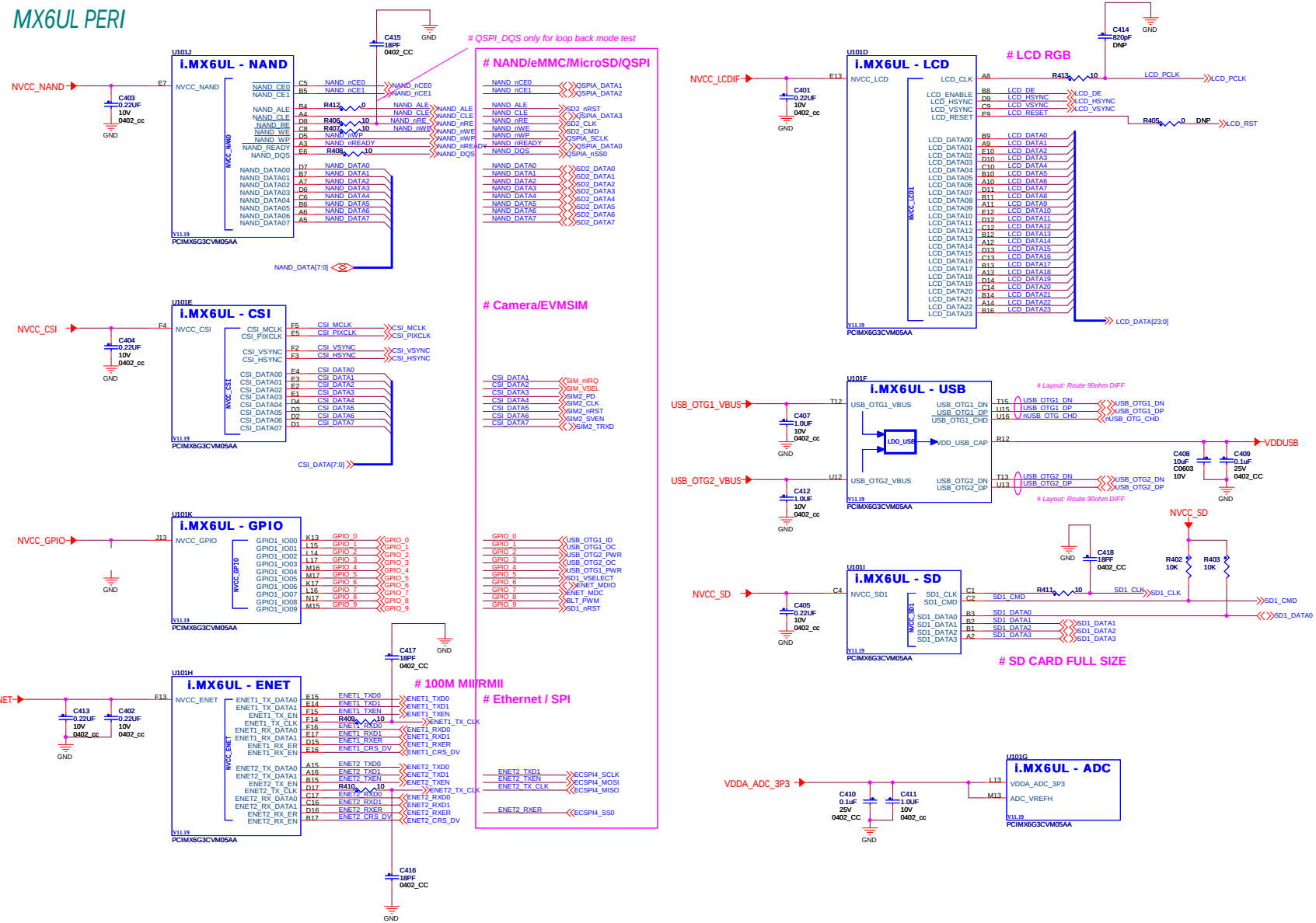
MX6UL PERI



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Title	CPU PERI1	
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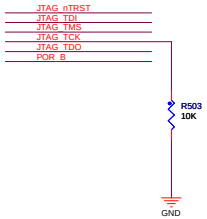
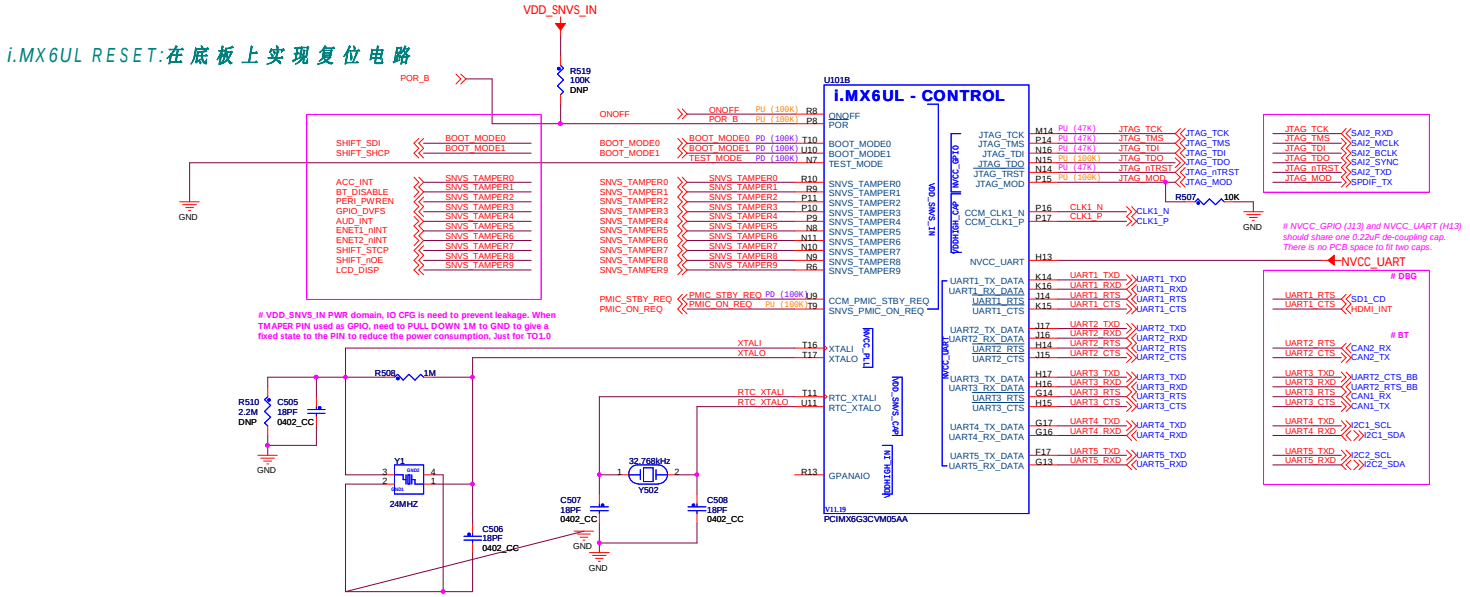
JTAG Debug



i.MX6UL RESET:在底板上实现复位电路



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FUSE MAP

<Default: QSPI BOOT>

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved		DDRSMP: "000" : Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Selection 0: select sampling at non-inverted clock 1: select sampling at inverted clock	HSDC: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0: select sampling at non-inverted clock 1: select sampling at inverted clock	FSDC: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11 - Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode SSM0: Preamble Delay, Read Latency: '0000' - 16 GPMICLK cycles. '0001' - 1 GPMICLK cycles. '0010' - 2 GPMICLK cycles. '0011' - 3 GPMICLK cycles. '1000' - 4 GPMICLK cycles. '1012' - 5 GPMICLK cycles. '1100' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

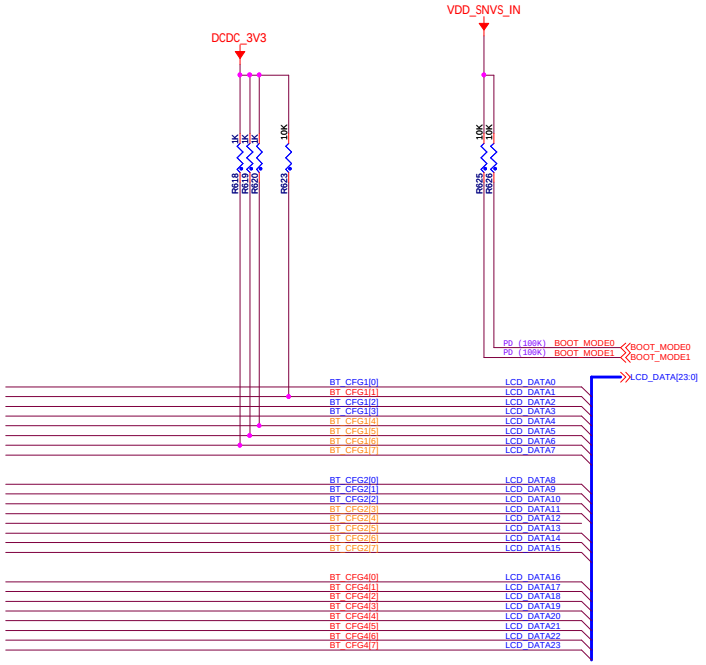
	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 -2-bytes (16-bit) 1 -3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	
0x460	L2_HW_INVALIDATE _DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/Emmc
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU _DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC IOMUX SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_IN (SD/MMC debug)	LPB_BOOT (Core / DDR Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

NAND MT29F32G08CBACA

1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= (1024K + 56K) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17,280Mb
1 LUN = 17,280Mb x 2 planes
= 34,560Mb

Boot Configuration

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



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Title: BOOT CFG

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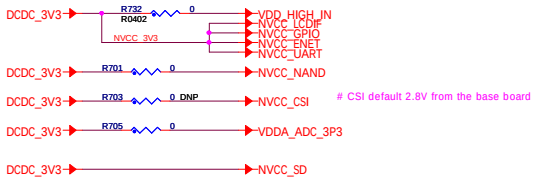
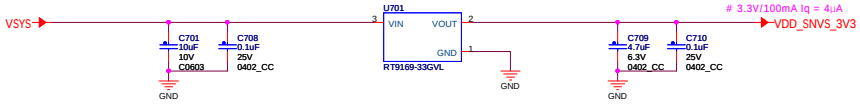
i.MX6UL PWR

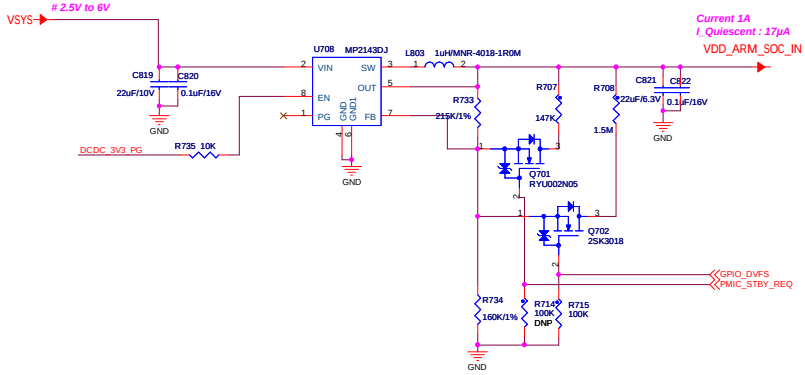
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				



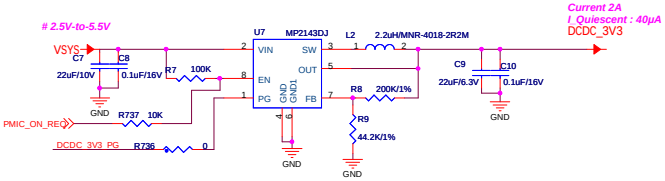
SNVS



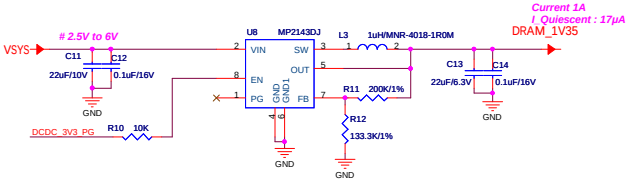
ARM/SOC



VDDHIGH / NVCC_xxx



LvDDR3



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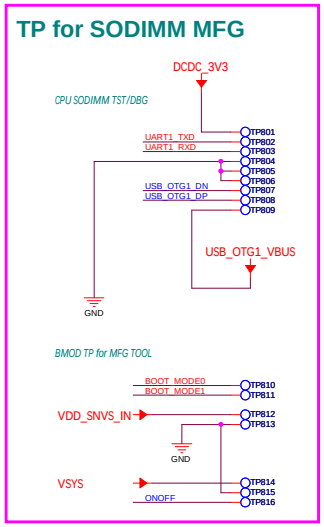
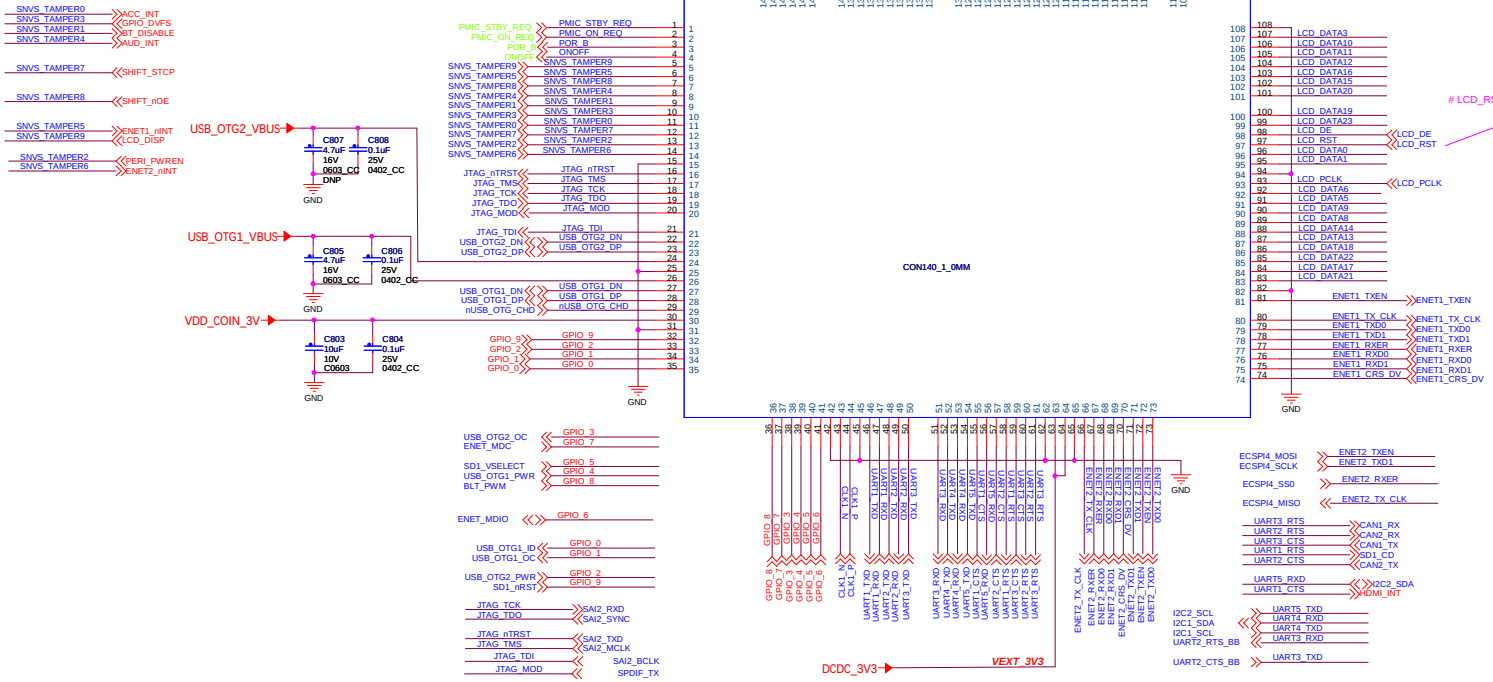
SODIMM 146

TP for SODIMM MFG





 # Maxim DCDC_3V3 supply current for Base Board: 1.2A

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Title	SODIMM	
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NOTE:

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1'b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)

i.MX6UL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	PAD DFU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									100K PD
POR_B	src.POR_B	src.POR_B									100K PU
ONOFF	src.RESET_B	src.RESET_B									100K PU
SNVS_PMIC_ON_REQ	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	snvs_lp_wrapper.PMIC_ON_REQ									100K PU
CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ	ccm.PMIC_VSTBY_REQ									100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]					gpio5.IO[10]				100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]					gpio5.IO[11]				100K PD
SNVS_TAMPER0	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[0]				Keeper
SNVS_TAMPER1	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[1]					gpio5.IO[1]				Keeper
SNVS_TAMPER2	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[2]				Keeper
SNVS_TAMPER3	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[3]					gpio5.IO[3]				Keeper
SNVS_TAMPER4	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[4]					gpio5.IO[4]				Keeper
SNVS_TAMPER5	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[5]				Keeper
SNVS_TAMPER6	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[6]				Keeper
SNVS_TAMPER7	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[7]					gpio5.IO[7]				Keeper
SNVS_TAMPER8	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[8]					gpio5.IO[8]				Keeper
SNVS_TAMPER9	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[9]					gpio5.IO[9]				Keeper
JTAG_MOD	sjc.MOD	sjc.MOD	gpt2.CLK	spdif.OUT	anatop.ENET_REF_CLK_25M	ccm.PMIC_RDY	gpio1.IO[10]	sdma.EXT_EVENT[0]			100K PU
JTAG_TMS	sjc.TMS	sjc.TMS	gpt2.CAPTURE1	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[11]	sdma.EXT_EVENT[1]		epit1.OUT	47K PU
JTAG_TDO	sjc.TDO	sjc.TDO	gpt2.CAPTURE2	sai2.TX_SYNC	ccm.CLKO2	ccm.STOP	gpio1.IO[12]	mqs.RIGHT		epit2.OUT	100K PU
JTAG_TDI	sjc.TDI	sjc.TDI	gpt2.COMPARE1	sai2.TX_BCLK	ccm.OUT0	pwm6.OUT	gpio1.IO[13]	mqs.LEFT		sim1.POWER_FAIL	47K PU
JTAG_TCK	sjc.TCK	sjc.TCK	gpt2.COMPARE2	sai2.RX_DATA	ccm.OUT1	pwm7.OUT	gpio1.IO[14]	osc32k.32K_OUT		sim2.POWER_FAIL	47K PU
JTAG_TRST_B	sjc.TRSTB	sjc.TRSTB	gpt2.COMPARE3	sai2.TX_DATA	ccm.OUT2	pwm8.OUT	gpio1.IO[15]	anatop.24M_OUT		caam_wrapper.RNG_OSC_OBS	47K PU
GPIO1_IO00	gpio1.IO[0]	i2c2.SCL	gpt1.CAPTURE1	anatop.OTG1_ID	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio1.IO[0]	enet1.1588_EVENT0_IN	src.SYSTEM_RESET	wdog3.WDOG_B	Keeper
GPIO1_IO01	gpio1.IO[1]	i2c2.SDA	gpt1.COMPARE1	usb.OTG1_OC	anatop.ENET_REF_CLK2	mqs.LEFT	gpio1.IO[1]	enet1.1588_EVENT0_OUT	src.EARLY_RESET	wdog1.WDOG_B	Keeper
GPIO1_IO02	gpio1.IO[2]	i2c1.SCL	gpt1.COMPARE2	usb.OTG2_PWR	anatop.ENET_REF_CLK_25M	usdhc1.WP	gpio1.IO[2]	sdma.EXT_EVENT[0]	src.ANY_PU_RESET	uart1.TX	Keeper
GPIO1_IO03	gpio1.IO[3]	i2c1.SDA	gpt1.COMPARE3	usb.OTG2_OC	osc32k.32K_OUT	usdhc1.CD_B	gpio1.IO[3]	ccm.DI0_EXT_CLK	src.TESTER_ACK	uart1.RX	Keeper
GPIO1_IO04	gpio1.IO[4]	anatop.ENET_REF_CLK1	pwm3.OUT	usb.OTG1_PWR	anatop.24M_OUT	usdhc1.RESET_B	gpio1.IO[4]	enet2.1588_EVENT0_IN	ccm.PLL2_BYP	uart5.TX	Keeper
GPIO1_IO05	gpio1.IO[5]	anatop.ENET_REF_CLK2	pwm4.OUT	anatop.OTG2_ID	csi.FIELD	usdhc1.VSELECT	gpio1.IO[5]	enet2.1588_EVENT0_OUT	ccm.PLL3_BYP	uart5.RX	Keeper
GPIO1_IO06	gpio1.IO[6]	enet1.MDIO	enet2.MDIO	usb.OTG_PWR_WAKE	csi.MCLK	usdhc2.WP	gpio1.IO[6]	ccm.WAIT	ccm.REF_EN_B	uart1.CTS_B	Keeper
GPIO1_IO07	gpio1.IO[7]	enet1.MDC	enet2.MDC	usb.OTG_HOST_MODE	csi.PIXCLK	usdhc2.CD_B	gpio1.IO[7]	ccm.STOP	ecspi1.TESTER_TRIGGER	uart1.RTS_B	Keeper
GPIO1_IO08	gpio1.IO[8]	pwm1.OUT	wdog1.WDOG_B	spdif.OUT	csi.VSYNC	usdhc2.VSELECT	gpio1.IO[8]	ccm.PMIC_RDY	ecspi2.TESTER_TRIGGER	uart5.RTS_B	Keeper
GPIO1_IO09	gpio1.IO[9]	pwm2.OUT	global wdog	spdif.IN	csi.HSYNC	usdhc2.RESET_B	gpio1.IO[9]	usdhc1.RESET_B	ecspi3.TESTER_TRIGGER	uart5.CTS_B	Keeper
UART1_TXD	gpio1.IO[16]	uart1.TX	enet1.RDATA[2]	i2c3.SCL	csi.DATA[2]	gpt1.COMPARE1	gpio1.IO[16]	anatop.USBPHY1_TSTI_TX_LS_MODE	ecspi4.TESTER_TRIGGER	spdif.OUT	Keeper
UART1_RXD	gpio1.IO[17]	uart1.RX	enet1.RDATA[3]	i2c3.SDA	csi.DATA[3]	gpt1.CLK	gpio1.IO[17]	anatop.USBPHY1_TSTI_TX_HS_MODE	usdhc1.TESTER_TRIGGER	spdif.IN	Keeper
UART1_CTS	gpio1.IO[18]	uart1.CTS_B	enet1.RX_CLK	usdhc1.WP	csi.DATA[4]	enet2.1588_EVENT1_IN	gpio1.IO[18]	anatop.USBPHY1_TSTI_TX_DN	usdhc2.TESTER_TRIGGER	usdhc2.WP	Keeper
UART1_RTS	gpio1.IO[19]	uart1.RTS_B	enet1.TX_ER	usdhc1.CD_B	csi.DATA[5]	enet2.1588_EVENT1_OUT	gpio1.IO[19]	anatop.USBPHY1_TSTO_RX_SQUELCH	qspi.TESTER_TRIGGER	usdhc2.CD_B	Keeper
UART2_TXD	gpio1.IO[20]	uart2.TX	enet1.TDATA[2]	i2c4.SCL	csi.DATA[6]	gpt1.CAPTURE1	gpio1.IO[20]	anatop.USBPHY1_TSTO_RX_DISCON_DET	rawnand.TESTER_TRIGGER	ecspi3.SS0	Keeper
UART2_RXD	gpio1.IO[21]	uart2.RX	enet1.TDATA[3]	i2c4.SDA	csi.DATA[7]	gpt1.CAPTURE2	gpio1.IO[21]	anatop.USBPHY1_TSTO_RX_HS_RXD	sjc.DONE	ecspi3.SCLK	Keeper
UART2_CTS	gpio1.IO[22]	uart2.CTS_B	enet1.CRS	can2.TX	csi.DATA[8]	gpt1.COMPARE2	gpio1.IO[22]	anatop.USBPHY2_TSTO_RX_FS_RXD	sjc.DE_B	ecspi3.MOSI	Keeper
UART2_RTS	gpio1.IO[23]	uart2.RTS_B	enet1.COL	can2.RX	csi.DATA[9]	gpt1.COMPARE3	gpio1.IO[23]	anatop.USBPHY1_TSTO_RX_FS_RXD	sjc.FAIL	ecspi3.MISO	Keeper
UART3_TXD	gpio1.IO[24]	uart3.TX	enet2.RDATA[2]	sim1.PORT0_PD	csi.DATA[1]	uart2.CTS_B	gpio1.IO[24]	anatop.USBPHY1_TSTI_TX_DP	sjc.JTAG_ACT	anatop.OTG1_ID	Keeper
UART3_RXD	gpio1.IO[25]	uart3.RX	enet2.RDATA[3]	sim2.PORT0_PD	csi.DATA[0]	uart2.RTS_B	gpio1.IO[25]	anatop.USBPHY1_TSTI_TX_EN	sim_m.HADDR[0]	epit1.OUT	Keeper
UART3_CTS	gpio1.IO[26]	uart3.CTS_B	enet2.RX_CLK	can1.TX	csi.DATA[10]	enet1.1588_EVENT1_IN	gpio1.IO[26]	anatop.USBPHY1_TSTI_TX_HIZ	sim_m.HADDR[1]	epit2.OUT	Keeper
UART3_RTS	gpio1.IO[27]	uart3.RTS_B	enet2.TX_ER	can1.RX	csi.DATA[11]	enet1.1588_EVENT1_OUT	gpio1.IO[27]	anatop.USBPHY2_TSTO_RX_HS_RXD	sim_m.HADDR[2]	wdog1.WDOG_B	Keeper
UART4_TXD	gpio1.IO[28]	uart4.TX	enet2.TDATA[2]	i2c1.SCL	csi.DATA[12]	csu.CSU_ALARM_AUT[2]	gpio1.IO[28]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	sim_m.HADDR[3]	ecspi2.SCLK	Keeper
UART4_RXD	gpio1.IO[29]	uart4.RX	enet2.TDATA[3]	i2c1.SDA	csi.DATA[13]	csu.CSU_ALARM_AUT[1]	gpio1.IO[29]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	sim_m.HADDR[4]	ecspi2.SS0	Keeper
UART5_TXD	gpio1.IO[30]	uart5.TX	enet2.CRS	i2c2.SCL	csi.DATA[14]	csu.CSU_ALARM_AUT[0]	gpio1.IO[30]	anatop.USBPHY2_TSTO_RX_SQUELCH	sim_m.HADDR[5]	ecspi2.MOSI	Keeper
UART5_RXD	gpio1.IO[31]	uart5.RX	enet2.COL	i2c2.SDA	csi.DATA[15]	csu.CSU_INT_DEB	gpio1.IO[31]	anatop.USBPHY2_TSTO_RX_DISCON_DET	sim_m.HADDR[6]	ecspi2.MISO	Keeper
ENET1_RXD0	gpio2.IO[0]	enet1.RDATA[0]	uart4.RTS_B	pwm1.OUT	csi.DATA[16]	can1.TX	gpio2.IO[0]	kpp.ROW[0]	sim_m.HADDR[7]	usdhc1.LCTL	Keeper
ENET1_RXD1	gpio2.IO[1]	enet1.RDATA[1]	uart4.CTS_B	pwm2.OUT	csi.DATA[17]	can1.RX	gpio2.IO[1]	kpp.COL[0]	sim_m.HADDR[8]	usdhc2.LCTL	Keeper
ENET1_CRS_DV	gpio2.IO[2]	enet1.RX_EN	uart5.RTS_B	osc32k.32K_OUT	csi.DATA[18]	can2.TX	gpio2.IO[2]	kpp.ROW[1]	sim_m.HADDR[9]	usdhc1.VSELECT	Keeper
ENET1_TXD0	gpio2.IO[3]	enet1.TDATA[0]	uart5.CTS_B	anatop.24M_OUT	csi.DATA[19]	can2.RX	gpio2.IO[3]	kpp.COL[1]	sim_m.HADDR[10]	usdhc2.VSELECT	Keeper
ENET1_TXD1	gpio2.IO[4]	enet1.TDATA[1]	uart6.CTS_B	pwm5.OUT	csi.DATA[20]	enet2.MDIO	gpio2.IO[4]	kpp.ROW[2]	sim_m.HADDR[11]	wdog1.WDOG_RST_B_DEB	Keeper
ENET1_TXEN	gpio2.IO[5]	enet1.TX_EN	uart6.RTS_B	pwm6.OUT	csi.DATA[21]	enet2.MDC	gpio2.IO[5]	kpp.COL[2]	sim_m.HADDR[12]	wdog2.WDOG_RST_B_DEB	Keeper
ENET1_TXCLK	gpio2.IO[6]	enet1.TX_CLK	uart7.CTS_B	pwm7.OUT	csi.DATA[22]	anatop.ENET_REF_CLK1	gpio2.IO[6]	kpp.ROW[3]	sim_m.HADDR[13]	gpt1.CLK	Keeper
ENET1_RXER	gpio2.IO[7]	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	csi.DATA[23]	weim.CRE	gpio2.IO[7]	kpp.COL[3]	sim_m.HADDR[14]	gpt1.CAPTURE2	Keeper
ENET2_RXD0	gpio2.IO[8]	enet2.RDATA[0]	uart6.TX	sim1.PORT0_TRXD	i2c3.SCL	enet1.MDIO	gpio2.IO[8]	kpp.ROW[4]	sim_m.HADDR[15]	usb.OTG1_PWR	Keeper
ENET2_RXD1	gpio2.IO[9]	enet2.RDATA[1]	uart6.RX	sim1.PORT0_CLK	i2c3.SDA	enet1.MDC	gpio2.IO[9]	kpp.COL[4]	sim_m.HADDR[16]	usb.OTG1_OC	Keeper
ENET2_CRS_DV	gpio2.IO[10]	enet2.RX_EN	uart7.TX	sim1.PORT0_RST_B	i2c4.SCL	weim.ADDR[26]	gpio2.IO[10]	kpp.ROW[5]	sim_m.HADDR[17]	anatop.ENET_REF_CLK_25M	Keeper
ENET2_TXD0	gpio2.IO[11]	enet2.TDATA[0]	uart7.RX	sim1.PORT0_SVEN	i2c4.SDA	weim.EB_B[2]	gpio2.IO[11]	kpp.COL[5]	sim_m.HADDR[18]	anatop.24M_OUT	Keeper
ENET2_TXD1	gpio2.IO[12]	enet2.TDATA[1]	uart8.TX	sim2.PORT0_TRXD	ecspi4.SCLK	weim.EB_B[3]	gpio2.IO[12]	kpp.ROW[6]	sim_m.HADDR[19]	usb.OTG2_PWR	Keeper
ENET2_TXEN	gpio2.IO[13]	enet2.TX_EN	uart8.RX	sim2.PORT0_CLK	ecspi4.MOSI	weim.ACLK_FREERUN	gpio2.IO[13]	kpp.COL[6]	sim_m.HADDR[20]	usb.OTG2_OC	Keeper
ENET2_TXCLK	gpio2.IO[14]	enet2.TX_CLK	uart8.CTS_B	sim2.PORT0_RST_B	ecspi4.MISO	anatop.ENET_REF_CLK2	gpio2.IO[14]	kpp.ROW[7]	sim_m.HADDR[21]	anatop.OTG2_ID	Keeper
ENET2_RXER	gpio2.IO[15]	enet2.RX_ER	uart8.RTS_B	sim2.PORT0_SVEN	ecspi4.SS0	weim.ADDR[25]	gpio2.IO[15]	kpp.COL[7]	sim_m.HADDR[22]	global wdog	Keeper
LCD_CLK	gpio3.IO[0]	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	weim.CS2_B	gpio3.IO[0]	ocotp_ctrl_wrapper.FUSE_LATCHED	sim_m.HADDR[23]	wdog1.WDOG_RST_B_DEB	Keeper
LCD_ENABLE	gpio3.IO[1]	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS3_B	gpio3.IO[1]	anatop.TESTI[0]	sim_m.HADDR[24]	ecspi2.RDY	Keeper
LCD_HSYNC	gpio3.IO[2]	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[2]	anatop.TESTI[1]	sim_m.HADDR[25]	ecspi2.SS1	Keeper
LCD_VSYNC	gpio3.IO[3]	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[3]	anatop.TESTI[2]	sim_m.HADDR[26]	ecspi2.SS2	Keeper
LCD_RESET	gpio3.IO[4]	lcdif.RESET	lcdif.CS	ca7_platform.EVENTI	sai3.TX_DATA	global wdog	gpio3.IO[4]	anatop.TESTI[3]	sim_m.HADDR[27]	ecspi2.SS3	Keeper
LCD_DATA00	gpio3.IO[5]	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[5]	src.BT_CFG[0]	sim_m.HADDR[28]	sai1.MCLK	Keeper
LCD_DATA01	gpio3.IO[6]	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[6]	src.BT_CFG[1]	sim_m.HADDR[29]	sai1.TX_SYNC	Keeper
LCD_DATA02	gpio3.IO[7]	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[7]	src.BT_CFG[2]	sim_m.HADDR[30]	sai1.TX_BCLK	Keeper
LCD_DATA03	gpio3.IO[8]	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[8]	src.BT_CFG[3]	sim_m.HADDR[31]	sai1.RX_DATA	Keeper
LCD_DATA04	gpio3.IO[9]	lcdif.DATA[4]	uart8.CTS_B	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	spdif.SR_CLK	gpio3.IO[9]	src.BT_CFG[4]	sim_m.HBURST[0]	sai1.TX_DATA	Keeper
LCD_DATA05	gpio3.IO[10]	lcdif.DATA[5]	uart8.RTS_B	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[10]	src.BT_CFG[5]	sim_m.HBURST[1]	ecspi1.SS1	Keeper
LCD_DATA06	gpio3.IO[11]	lcdif.DATA[6]	uart7.CTS_B	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[11]	src.BT_CFG[6]	sim_m.HBURST[2]	ecspi1.SS2	Keeper
LCD_DATA07	gpio3.IO[12]	lcdif.DATA[7]	uart7.RTS_B	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[12]	src.BT_CFG[7]	sim_m.HMASTLOCK	ecspi1.SS3	Keeper
LCD_DATA08	gpio3.IO[13]	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[13]	src.BT_CFG[8]	sim_m.HPROT[0]	can1.TX	Keeper
LCD_DATA09	gpio3.IO[14]	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[14]	src.BT_CFG[9]	sim_m.HPROT[1]	can1.RX	Keeper
LCD_DATA10	gpio3.IO[15]	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[15]	src.BT_CFG[10]	sim_m.HPROT[2]	can2.TX	Keeper
LCD_DATA11	gpio3.IO[16]	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[16]	src.BT_CFG[11]	sim_m.HPROT[3]	can2.RX	Keeper
LCD_DATA12	gpio3.IO[17]	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[17]	src.BT_CFG[12]	sim_m.HREADYOUT	ecspi1.RDY	Keeper
LCD_DATA13	gpio3.IO[18]	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	sim_m.HRESP	usdhc2.RESET_B	Keeper
LCD_DATA14	gpio3.IO[19]	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	sim_m.HSIZE[0]	usdhc2.DATA4	Keeper
LCD_DATA15	gpio3.IO[20]	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[20]	src.BT_CFG[15]	sim_m.HSIZE[1]	usdhc2.DATA5	Keeper
LCD_DATA16	gpio3.IO[21]	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[21]	src.BT_CFG[24]	sim_m.HSIZE[2]	usdhc2.DATA6	Keeper
LCD_DATA17	gpio3.IO[22]	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[22]	src.BT_CFG[25]	sim_m.HWRITE	usdhc2.DATA7	Keeper
LCD_DATA18	gpio3.IO[23]	lcdif.DATA[18]	pwm5.OUT	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[23]	src.BT_CFG[26]	tpsmp.CLK	usdhc2.CMD	Keeper
LCD_DATA19	gpio3.IO[24]	lcdif.DATA[19]	pwm6.OUT	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[24]	src.BT_CFG[27]	tpsmp.HDATA_DIR	usdhc2.CLK	Keeper
LCD_DATA20	gpio3.IO[25]	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[25]	src.BT_CFG[28]	tpsmp.HTRANS[0]	usdhc2.DATA0	Keeper
LCD_DATA21	gpio3.IO[26]	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[26]	src.BT_CFG[29]	tpsmp.HTRANS[1]	usdhc2.DATA1	Keeper
LCD_DATA22	gpio3.IO[27]	lcdif.DATA[22]	mqs.RIGHT	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[27]	src.BT_CFG[30]	tpsmp.HDATA[0]	usdhc2.DATA2	Keeper
LCD_DATA23	gpio3.IO[28]	lcdif.DATA[23]	mqs.LEFT	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[28]	src.BT_CFG[31]	tpsmp.HDATA[1]	usdhc2.DATA3	Keeper
NAND_RE_B	gpio4.IO[0]	rawnand.RE_B	usdhc2.CLK	qspiB_SCLK	kpp.ROW[0]	weim.EB_B[0]	gpio4.IO[0]	anatop.TESTO[0]	tpsmp.HDATA[2]	ecspi3.SS2	Keeper
NAND_WE_B	gpio4.IO[1]	rawnand.WE_B	usdhc2.CMD	qspiB_SS0_B	kpp.COL[0]	weim.EB_B[1]	gpio4.IO[1]	anatop.TESTO[1]	tpsmp.HDATA[3]	ecspi3.SS3	Keeper
NAND_DATA00	gpio4.IO[2]	rawnand.DATA00	usdhc2.DATA0	qspiB_SS1_B	kpp.ROW[1]	weim.AD[8]	gpio4.IO[2]	anatop.TESTO[2]	tpsmp.HDATA[4]	ecspi4.RDY	Keeper
NAND_DATA01	gpio4.IO[3]	rawnand.DATA01	usdhc2.DATA1	qspiB_DQS	kpp.COL[1]	weim.AD[9]	gpio4.IO[3]	anatop.TESTO[3]	tpsmp.HDATA[5]	ecspi4.SS1	Keeper
NAND_DATA02	gpio4.IO[4]	rawnand.DATA02	usdhc2.DATA2	qspiB_DATA[0]	kpp.ROW[2]	weim.AD[10]	gpio4.IO[4]	anatop.TESTO[4]	tpsmp.HDATA[6]	ecspi4.SS2	Keeper
NAND_DATA03	gpio4.IO[5]	rawnand.DATA03	usdhc2.DATA3	qspiB_DATA[1]	kpp.COL[2]	weim.AD[11]	gpio4.IO[5]	anatop.TESTO[5]	tpsmp.HDATA[7]	ecspi4.SS3	Keeper
NAND_DATA04	gpio4.IO[6]	rawnand.DATA04	usdhc2.DATA4	qspiB_DATA[2]	ecspi4.SCLK	weim.AD[12]	gpio4.IO[6]	anatop.TESTO[6]	tpsmp.HDATA[8]	uart2.TX	Keeper
NAND_DATA05	gpio4.IO[7]	rawnand.DATA05	usdhc2.DATA5	qspiB_DATA[3]	ecspi4.MOSI	weim.AD[13]	gpio4.IO[7]	anatop.TESTO[7]	tpsmp.HDATA[9]	uart2.RX	Keeper
NAND_DATA06	gpio4.IO[8]	rawnand.DATA06	usdhc2.DATA6	sai2.RX_BCLK	ecspi4.MISO	weim.AD[14]	gpio4.IO[8]	anatop.TESTO[8]	tpsmp.HDATA[10]	uart2.CTS_B	Keeper
NAND_DATA07	gpio4.IO[9]	rawnand.DATA07	usdhc2.DATA7	qspiA_SS1_B	ecspi4.SS0	weim.AD[15]	gpio4.IO[9]	anatop.TESTO[9]	tpsmp.HDATA[11]	uart2.RTS_B	Keeper
NAND_ALE	gpio4.IO[10]	rawnand.ALE	usdhc2.RESET_B	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[10]	anatop.TESTO[10]	tpsmp.HDATA[12]	ecspi3.SS1	Keeper
NAND_WP_B	gpio4.IO[11]	rawnand.WP_B	usdhc1.RESET_B	qspiA_SCLK	pwm4.OUT	weim.BCLK	gpio4.IO[11]	anatop.TESTO[11]	tpsmp.HDATA[13]	ecspi3.RDY	Keeper
NAND_READY_B	gpio4.IO[12]	rawnand.READY_B	usdhc1.DATA4	qspiA_DATA[0]	ecspi3.SS0	weim.CS1_B	gpio4.IO[12]	anatop.TESTO[12]	tpsmp.HDATA[14]	uart3.TX	Keeper
NAND_CE0_B	gpio4.IO[13]	rawnand.CE0_B	usdhc1.DATA5	qspiA_DATA[1]	ecspi3.SCLK	weim.DTACK_B	gpio4.IO[13]	anatop.TESTO[13]	tpsmp.HDATA[15]	uart3.RX	Keeper
NAND_CE1_B	gpio4.IO[14]	rawnand.CE1_B	usdhc1.DATA6	qspiA_DATA[2]	ecspi3.MOSI	weim.ADDR[18]	gpio4.IO[14]	anatop.TESTO[14]	tpsmp.HDATA[16]	uart3.CTS_B	Keeper
NAND_CLE	gpio4.IO[15]	rawnand.CLE	usdhc1.DATA7	qspiA_DATA[3]	ecspi3.MISO	weim.ADDR[16]	gpio4.IO[15]	anatop.TESTO[15]	tpsmp.HDATA[19]	uart3.RTS_B	Keeper
NAND_DQS	gpio4.IO[16]	rawnand.DQS	csi.FIELD	qspiA_SS0_B	pwm5.OUT	weim.WAIT	gpio4.IO[16]	sdma.EXT_EVENT[1]	tpsmp.HDATA[17]	spdif.EXT_CLK	Keeper
SD1_CMD	gpio2.IO[16]	usdhc1.CMD	gpt2.COMPARE1	sai2.RX_SYNC	spdif.OUT	weim.ADDR[19]	gpio2.IO[16]	sdma.EXT_EVENT[0]	tpsmp.HDATA[18]	usb.OTG1_PWR	Keeper
SD1_CLK	gpio2.IO[17]	usdhc1.CLK	gpt2.COMPARE2	sai2.MCLK	spdif.IN	weim.ADDR[20]	gpio2.IO[17]	ccm.OUT0	observe_mux.OUT[0]	usb.OTG1_OC	Keeper
SD1_DATA0	gpio2.IO[18]	usdhc1.DATA0	gpt2.COMPARE3	sai2.TX_SYNC	can1.TX	weim.ADDR[21]	gpio2.IO[18]	ccm.OUT1	observe_mux.OUT[1]	anatop.OTG1_ID	Keeper
SD1_DATA1	gpio2.IO[19]	usdhc1.DATA1	gpt2.CLK	sai2.TX_BCLK	can1.RX	weim.ADDR[22]	gpio2.IO[19]	ccm.OUT2	observe_mux.OUT[2]	usb.OTG2_PWR	Keeper
SD1_DATA2	gpio2.IO[20]	usdhc1.DATA2	gpt2.CAPTURE1	sai2.RX_DATA	can2.TX	weim.ADDR[23]	gpio2.IO[20]	ccm.CLKO1	observe_mux.OUT[3]	usb.OTG2_OC	Keeper
SD1_DATA3	gpio2.IO[21]	usdhc1.DATA3	gpt2.CAPTURE2	sai2.TX_DATA	can2.RX	weim.ADDR[24]	gpio2.IO[21]	ccm.CLKO2	observe_mux.OUT[4]	anatop.OTG2_ID	Keeper
CSI_MCLK	gpio4.IO[17]	csi.MCLK	usdhc2.CD_B	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio4.IO[17]	snvs_hp_wrapper.VIO_5_CTL	tpsmp.HDATA[20]	uart6.TX	Keeper
CSI_PIXCLK	gpio4.IO[18]	csi.PIXCLK	usdhc2.WP	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[18]	snvs_hp_wrapper.VIO_5	tpsmp.HDATA[21]	uart6.RX	Keeper
CSI_VSYNC	gpio4.IO[19]	csi.VSYNC	usdhc2.CLK	sim1.PORT1_CLK	i2c2.SDA	weim.RW	gpio4.IO[19]	pwm7.OUT	tpsmp.HDATA[22]	uart6.RTS_B	Keeper
CSI_HSYNC	gpio4.IO[20]	csi.HSYNC	usdhc2.CMD	sim1.PORT1_PD	i2c2.SCL	weim.LBA_B	gpio4.IO[20]	pwm8.OUT	tpsmp.HDATA[23]	uart6.CTS_B	Keeper
CSI_DATA00	gpio4.IO[21]	csi.DATA[2]	usdhc2.DATA0	sim1.PORT1_RST_B	ecspi2.SCLK	weim.AD[0]	gpio4.IO[21]	src.INT_BOOT	tpsmp.HDATA[24]	uart5.TX	Keeper
CSI_DATA01	gpio4.IO[22]	csi.DATA[3]	usdhc2.DATA1	sim1.PORT1_SVEN	ecspi2.SS0	weim.AD[1]	gpio4.IO[22]	sai1.MCLK	tpsmp.HDATA[25]	uart5.RX	Keeper
CSI_DATA02	gpio4.IO[23]	csi.DATA[4]	usdhc2.DATA2	sim1.PORT1_TRXD	ecspi2.MOSI	weim.AD[2]	gpio4.IO[23]	sai1.RX_SYNC	tpsmp.HDATA[26]	uart5.RTS_B	Keeper
CSI_DATA03	gpio4.IO[24]	csi.DATA[5]	usdhc2.DATA3	sim2.PORT1_PD	ecspi2.MISO	weim.AD[3]	gpio4.IO[24]	sai1.RX_BCLK	tpsmp.HDATA[27]	uart5.CTS_B	Keeper
CSI_DATA04	gpio4.IO[25]	csi.DATA[6]	usdhc2.DATA4	sim2.PORT1_CLK	ecspi1.SCLK	weim.AD[4]	gpio4.IO[25]	sai1.TX_SYNC	tpsmp.HDATA[28]	usdhc1.WP	Keeper
CSI_DATA05	gpio4.IO[26]	csi.DATA[7]	usdhc2.DATA5	sim2.PORT1_RST_B	ecspi1.SS0	weim.AD[5]	gpio4.IO[26]	sai1.TX_BCLK	tpsmp.HDATA[29]	usdhc1.CD_B	Keeper
CSI_DATA06	gpio4.IO[27]	csi.DATA[8]	usdhc2.DATA6	sim2.PORT1_SVEN	ecspi1.MOSI	weim.AD[6]	gpio4.IO[27]	sai1.RX_DATA	tpsmp.HDATA[30]	usdhc1.RESET_B	Keeper
CSI_DATA07	gpio4.IO[28]	csi.DATA[9]	usdhc2.DATA7	sim2.PORT1_TRXD	ecspi1.MISO	weim.AD[7]	gpio4.IO[28]	sai1.TX_DATA	tpsmp.HDATA[31]	usdhc1.VSELECT	Keeper